Parallel Printer Port for Phase Measurement

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***Abstract*-This white paper talks about the measurement of phase angle using Phase Locked Loop and printer port.. The phase detector compares the phase of a periodic input signal against the phase of the output of voltage controlled oscillator and generates an average output voltage V_{out} which is linearly proportional to the phase difference, $\Delta\phi$ between its two inputs. This output voltage is measured using the parallel Printer port of a PC.**

Keywords: Phase detector, voltage controlled oscillator, phase locked loop and parallel printer port.

I. INTRODUCTION

The recent developments of telecommunication systems has brought an increased demand for low-jitter, high-speed phase-locked loops (PLL). The phase detector is a key element in PLL's and has from a historical point of view not been able to handle large input frequency differences [1]. The phase detector compares the phase of a periodic input signal against the phase of the output of VCO, and generates an average output voltage $V_{out,}$ which is linearly proportional to the phase difference, $\Delta\phi$, between its two inputs. In the ideal case, the relationship between V_{out} and $\Delta\phi$ is linear, crossing the origin for $\Delta\phi = 0$ [2,3]. The output frequency of the VCO is directly proportional to input DC level. The VCO frequency is compared with the input frequency and adjusted until it is equal to the input frequency.

In short the PLL works in three states: free running, capture and phase lock. Before input is applied the PLL is in free running state. Once input is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continues to change until it is equal to the input frequency and phase locked state is obtained. When phase locked, the loop tracks any change in the input frequency through its repetitive action. In many applications the dynamic characteristics of PLL play an important role, mainly in the reduction of acquisition time and improvement in noise immunity.

A PLL operate on the same principle that the quantity fed back and compared is not the amplitude but the phase. VCO adjusts its own frequency until it is equal to that of input sinusoidal signal. At this point the frequency and phase of the signal are in synchronism[4].

PLL has emerged as one of the fundamental building block in electronics technology. The PLL principle is used in FM demodulators, frequency synthesized transmitters and receivers, FSK decoders for the generation of local oscillator frequency.

Phase sensitive detection technique is also used in two terminal ac measurements [5-8]. Phase sensitive detectors were used by Szaro [9] to perform conductance measurements over a wide band of frequency.To measure the phase introduced by capacitors Bruce & West [10] used phase meters. They have used this to analyse the ac conductivity of solid electrolyte in terms of equivalent circuits consisting of resistors and capacitors. Balaya and Sunandana [11] designed an electronic system based on quadrature oscillator and phase sensitive detection for measurement of ac conductivity .

To measure the phase difference between 2 signals upto frequency of 2.5 GHz Cowles and Gilbert [12] used AD8308. From the review of above literature it is evident that most of the available circuits are quite complex. In this work a modest attempt is made to develop a low cost simple circuit for the measurement of phase difference.

Most personal computers today are equipped with a parallel port commonly used to connect the computer to a parallel printer. Because it is available on most personal computers, the parallel port is a perfect choice for connection to other peripheral devices. However, communication to peripherals across the parallel port is limited because the interface is traditionally undirectional and there is no standard specification for the interface.

Additionally, although the performance of the personal computer has dramatically increased, the parallel port has remained the same.

II. EXPERIMENTAL SETUP

Phase locked loop IC is used to detect the phase introduced by the sample. Though there are many phase detectors like diode phase detector, double balanced phase detector etc., phase locked loop is preferred with a view to convert the phase into proportional dc voltage and proportional frequency within a single chip [13,14] . The block diagram is shown in Fig.1.

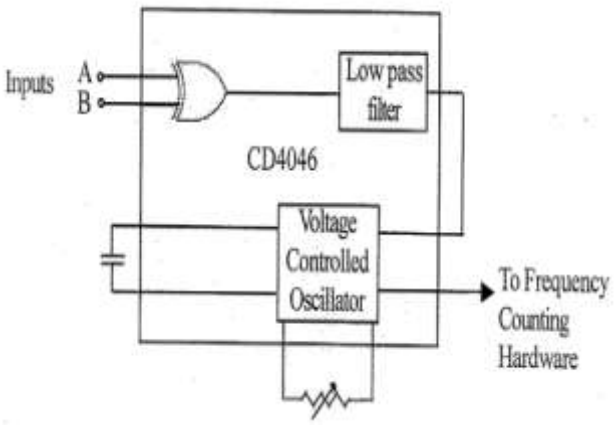

Fig.1. Block diagram of PLL

The IC used here is CD 4046 micropower phase locked loop. It consists of an exclusive OR gate, lowpase filter and a voltage controlled oscillator.

One of the basic and important components of a PLL is the voltage controlled oscillator [15 ,16].The inputs to XOR gate are the outputs from comparators. It produces an output voltage which has a dc component proportional to the phase difference between the input signals, which consists of a dc term and some ac components of input frequency.

The output of low pass filter has dc component, the magnitude of which is a function of the phase angle between two input signals. Voltage controlled oscillator converts the dc voltage from low pass filter into proportional frequency.

If the frequency of input signal changes, a change in phase angle between input signals will produce a change in dc voltage in such a manner as to vary the frequency of voltage controlled oscillator [17]. This change in frequency is measured with the help of frequency counter.

The frequency measuring hardware make use of three stages of 3-tier ICs consisting of 74LS393 (Dual 4-bit binary ripple counter), 74LS374 (8-bit positive edge triggered latch) and 74LS258 (Quad 2-line to 1-line Data Selector/Multiplexer). The counting and frequency measuring hardware is shown in Fig. 2.

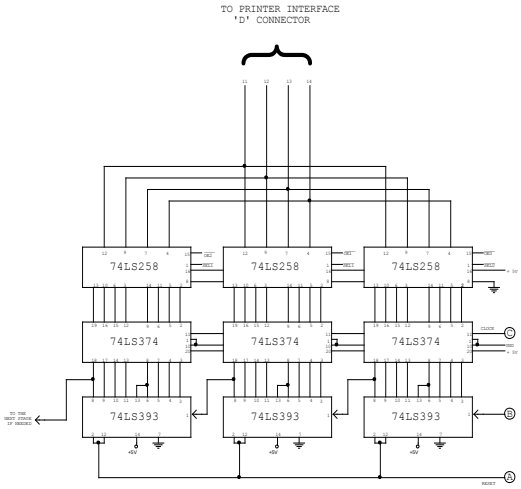

Fig.2.Counting and Frequency measuring circuit

The 3-tier ICs were cascaded to give a 3-stage counting system. Such a system can be used as a frequency counter by handling the signal such as resetting, counting, latching and reading properly. This synchronized behaviour was achieved by using 1 Hz signal in conjunction with logic gates (for gating arrangement) and monoshots to derive the necessary signal [18]. The hardware developed in achieving the above mentioned signals is described below.

To count the incoming pulses, IC 74LS393 was used. It is a dual 4-bit binary ripple counter.. The clock input to the first stage 74LS393 was obtained from the output of an AND gate.

Before the counting starts, all the counters were reset simultaneously to make it ready for counting the pulses. The AND gate was disabled after 1 Sec. Thus, the count registered directly gives the frequency. One can also use IC 74LS161 instead of 74LS393, which can generate a look-ahead carry for faster counting.

The pulses counted have to be latched for reading and before starting of the next cycle. IC 74LS374 was used for this purpose. The outputs of these latches were always enabled. The signal from the monoshot was fed to the cascaded clock-input of the latches. This signal will transfer the date appearing at the input of the latches.

Reading of the data latched at the outputs of 74LS374s was done by the PC. Infact, the 24-bit count appearing at the output of 74LS374 needs three 8-bit ports. Simultaneous reading of 24 bits calls for an add-on card such as digital input output (DIO) card having two 8255s. Further, mounting of such a card on the slot of the motherboard needs the PC to be opened.[19,20].

In the present work, advantage is taken of the Centronics printer port (available at the rear of the PC) to read the register counts (frequency) sequentially [21]. The PC AT (80383 SX) used in the present work had two printer ports: LPT1 and LPT2. One of these ports was used for reading the frequency.

III. EXPERIMENTAL PROCEDURE

The measurement of phase difference between two signals of same frequency was carried out by various methods. The new method adopted in this work is a frequency conversion method using phase locked loop IC CD 4046. The block diagram of the method used is shown in Fig1. The zero crossing detectors convert the input signals into square pulses, which were fed to XOR phase detector.

The XOR gate output voltage has a dc component proportional to phase difference between the input signals. The output of the phase detector was fed to a low pass filter to remove high frequency components. The output dc voltage from the low pass filter was fed as input to the linear voltage controlled oscillator.

The VCO frequency was determined by VR and C values and the maximum frequency was set to 180 kHz, which corresponds to 180^0 phase shift. When the phase difference between the two input signals was 90^0, the VCO output was 90 kHz. Thus the output frequency was directly proportional to the input phase difference.

The scheme was built and tested with a CMOS micro PLL chip CD 4046. It was found that the scheme needs calibration for different frequency settings before a fruitful measurement is made. However, the calibration can be

easily achieved with the help of an inverting amplifier and the variable resistor VR. Before making a measurement, the inputs to XOR were fed from one of the signals and its inverted output employing an inverting amplifier.

It maintains a constant 180^0 phase difference between the two input signals A and B. VR was now adjusted to set the VCO output frequency to 180 kHz. The output of the VCO(X) was fed to the frequency measuring unit .

IV. RESULTS AND DISCUSSION

In order to study the reliability and repeatability of the steup we have used some standard capacitors to introduce the phase difference between the two inputs given to an X-OR gate.

The phase difference obtained theoretically and experimentally is found to be in quiet good agreement. This low cost simple technique can be employed to carry out phase measurements in unknown samples. From this phase angle , one can determine ac conductivity.

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