

Efficient Implementation of Sample Rate Converter

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Abstract—Within wireless base station system design, manufacturers continue to seek ways to add value and performance while increasing differentiation. Transmit/receive functionality has become an area of focus as designers attempt to address the need to move data from very high frequency sample rates to chip processing rates. Digital Up Converter (DUC) and Digital Down Converter (DDC) are used as sample rate converters. These are the important block in every digital communication system; hence there is a need for effective implementation of sample rate converter so that cost can be reduced. With the recent advances in FPGA technology, the more complex devices providing high-speed as required in DSP applications are available. The filter implementation in FPGA, utilizing the dedicated hardware resources can effectively achieve application-specific integrated circuit (ASIC)-like performance while reducing development time cost and risks. So in this paper the technique for an efficient design of DDC for reducing sample rate is being suggested which meets the specifications of WiMAX system. Its effective implementation also ensures the pathway for the efficient applications in VLSI designs. Different design configurations for the sample rate converter are explored. The sample rate converter can be designed using half band filters, fixed FIR filters, poly-phase filters, CIC filters or even farrow filters.

Keywords: WiMAX; Half Band filter; FIR filter; CIC Filter; Farrow Filter; FPGA.

I. INTRODUCTION

Sample rate conversion (SRC) is the process of changing the sampling rate of a data stream from a specific sampling rate (e.g. the input/output hardware rate) to another sampling rate (e.g. the application rate). With the conversion of communication and software markets, SRC is becoming a necessary component in many of today's applications including Digital Mixing Consoles and Digital Audio Workstations, CD-R, MD Recorders, Multitrack Digital Audio and Video Tape Recorders, Digital Audio Broadcast Equipment, Digital Tape Recorders, Computer Communication and Multimedia Systems. In most of these applications, a very high quality sample rate converter is required. Most high quality SRCs currently available on the market employ a digital filter that provides the required quality by up-sampling the data to a very high sampling rate followed by down-sampling to the required output sampling rate. The digital filters have also emerged as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architectures. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog

filters. The Cascaded Integrator Comb (CIC) filter is a digital filter which is employed for multiplier-less realization. This type of filter has extensive applications in low-cost implementation of interpolators and decimators. However, there is a problem of pass-band droop, which can be eliminated using compensation techniques. The Farrow filters is another class of digital filters which are used extensively in arbitrary sample rate conversions and fractionally delaying the samples. They have poly-phase structure and are very efficient for digital filtering. In addition to this, Field-Programmable gate Array (FPGA) has become an extremely cost-effective means of off-loading computationally intensive digital signal processing algorithms to improve overall system performance.

In this paper for Sample Rate Converter, CIC filter with and without compensation technique are implemented on FPGA. Farrow filters are also implemented for fractional delay and arbitrary change in sample rate conversion. Both of these filter configurations provide a better performance than the common filter structures in terms of speed of operation, cost, and power consumption in real-time. These filters are implemented in Altera Stratix-II-EP2S15F484C3 FPGA and simulated with the help of Quartus II v9.1sp2.

A. Cascaded Integrator Comb (CIC) Filters

The CIC filter is a multiplier free filter that can handle large rate changes. It was proposed by Eugene Hogenauer in 1981 [1]. It is formed by integrating basic 1-bit integrators and 1-bit differentiators. It uses limited storage as it can be constructed using just adders and delay elements. That's why it is also well suited for FPGA and ASIC implementation. The CIC filter can also be implemented very efficiently in hardware due to its symmetric structure.

The CIC filter is a combination of digital integrator and digital differentiator stages, which can perform the operation of digital low pass filtering and decimation at the same time. The transfer function of the CIC filter in z-domain is given in equation (1) [1].

$$H(z) = \left(\frac{1 - z^{-K}}{1 - z^{-1}} \right)^L \quad (1)$$

In equation (1), K is the oversampling ratio and L is the order of the filter. The numerator $(1 - z^{-K})$ represents the transfer function of a differentiator and the denominator $(1/(1 - z^{-1}))^L$ indicates the transfer function of an integrator.

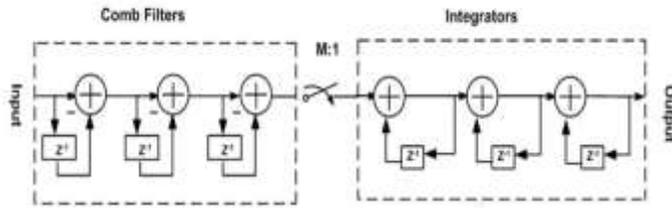


Figure 1: CIC Filter [2]

The CIC filter first performs the averaging operation then follows it with the decimation. A simple block diagram of a first order CIC filter is shown in Figure 1. Here the clock divider divides the oversampling clock signal by the oversampling ratio, M after the integrator stage. The same output can be achieved by having the decimation stage between integrator stage and comb stage. By dividing the clock frequency by M the delay buffer depth requirement of the comb section is reduced. In Figure 1, the integrator operates at the sampling clock frequency, while the differentiator operates at down sampled clock frequency of f_s/M . By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved.

A very poor magnitude characteristic of the comb filter is improved by cascading several identical comb filters. The transfer function $H(z)$ of the multistage comb filter composed of K identical single stage comb filters is given by

$$H(z) = \left(\frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}} \right)^K \quad (2)$$

Figure 2 shows how the multistage realization improves the selectivity and the stop-band attenuation of the overall filter: the selectivity and the stop-band attenuation are augmented with the increase of the number of comb filter sections. The filter has multiple nulls with multiplicity equal to the number of the sections (K). Consequently, the stop-band attenuation in the null intervals is very high. Figure 3 illustrates a monotonic decrease of the magnitude response in the pass-band, called the pass-band droop.

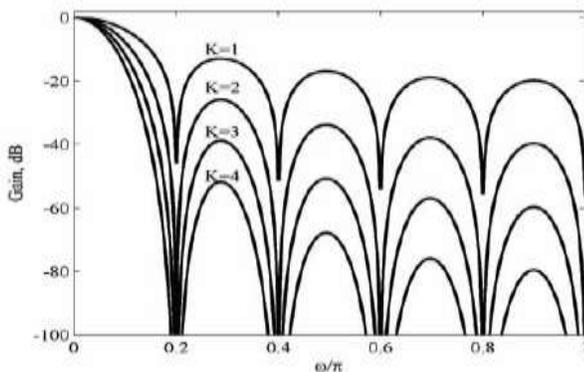


Figure 2: CIC filter gain responses: single-stage $K=1$, two-stage $K=2$, three-stage $K=3$ and four-stage $K=4$. [3]

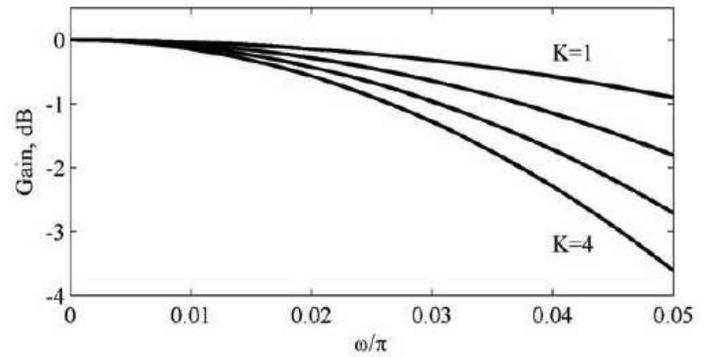


Figure 3: CIC Filter Gain Response: Pass-band Droop for Figure 2. [3]

B. CIC filter for sample rate conversion

The CIC filters are utilized in multirate systems for constructing digital Upconverter and Downconverter. The ability of comb filter to perform filtering without multiplications is very attractive to be applied to high rate signals. Moreover, CIC filters are convenient for large conversion factors since the low-pass bandwidth is very small. In multistage decimators with a large conversion factor, the comb filter is the best solution for the first decimation stage, whereas in interpolators, the comb filter is convenient for the last interpolation stage.

C. CIC filters for Decimators

The basic concept of a CIC decimator is explained in Figure 4. Figure 4(a) shows the factor-of- N decimator consisting of the K -stage CIC filter and the factor-of- N down-sampler. Applying the third identity, the factor-of- N down-sampler is moved and placed behind the integrator section and before the comb section; see Figure 4(b). Finally, the CIC decimator is implemented as a cascade of K integrators, factor-of- N down-sampler, and the cascade of K differentiator (comb) sections. The integrator portion operates at the input data rate, whereas the differentiator (comb) portion operates at the N times lower sampling rate.

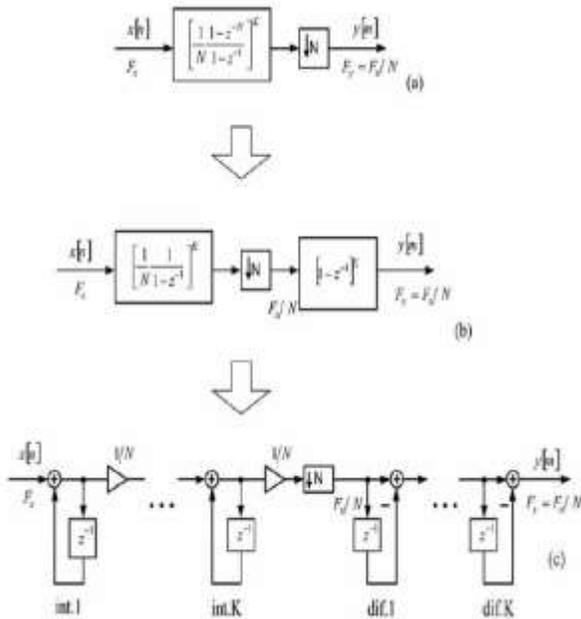


Figure 4: Block diagram representation of CIC decimator:
 (a) Cascade of CIC filter and down-sampler.
 (b) Cascade of integrator section, down-sampler, and comb section.
 (c) Implementation structure consisting of the cascade of K integrators, down sampler, and the cascade of K differentiators. [3]

D. CIC filters in Interpolators

The basic concept of a CIC interpolator is shown in Figure 5. Figure 5 (a) depicts the factor-of-N interpolator consisting of the factor-of-N up-sampler and the K-stage CIC filter. Applying the sixth identity, the factor-of-N up-sampler is moved and placed behind the differentiator (comb) section and before the integrator section; see Figure 5 (b). Finally, the CIC interpolator is implemented as a cascade of K differentiator (comb) sections, factor-of-N down-sampler, and the cascade of K integrators. The comb portion operates at the input data rate, whereas the integrator portion operates at the N times higher sampling rate.

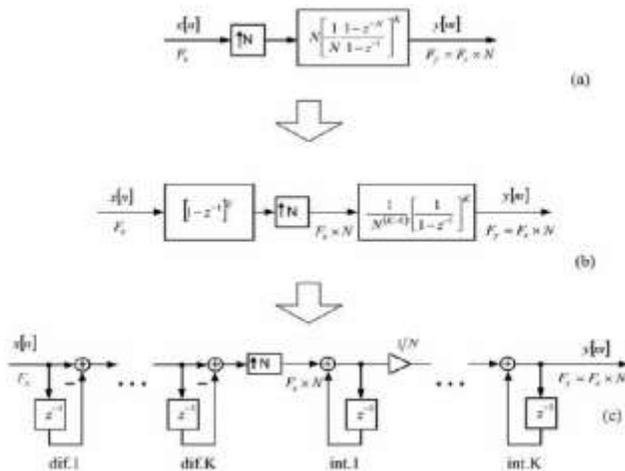


Figure 5: Block diagram representation of CIC interpolator:

- (a) Cascade of up-sampler and CIC filter.
- (b) Cascade of comb section, down-sampler, and integrator section.
- (c) Implementation structure consisting of the cascade of K differentiators, down sampler, and the cascade of K integrators. [3]

The configuration composed as a cascade of interpolators and differentiators (differentiators and interpolators) separated by a down-sampler (up-sampler) is called recursive realization structure, or a CIC realization structure. The advantage of CIC decimators and interpolators is the ability of sampling rate conversion without multiplying operations. This is of particular interest when operating at high frequencies. Considering the implementation aspects of CIC filters, one should expect the register overflow, since the integrator has a unity feedback. Actually, the register overflow is a reality in all integrator stages. It is shown that the register overflow is of no consequence if the two's complement arithmetic is used and the range of the number system is equal to or exceeds the maximum magnitude expected at the output of the composite filter. In order to avoid register overflow in the integrator section, the word-length has to be equal to or greater than

$(W_0 + K \log_2 N)$ bits, where W_0 is the word-length in bits of the input signal.

E. CIC filters in decimation and interpolation

A CIC filter can be used as a first stage in decimation when the overall conversion ratio M is factorable as

$$M = N \times R \quad (3)$$

The overall factor-of-M sampling rate conversion system can be implemented by cascading a factor-of-N CIC decimator and a factor-of-R FIR decimator as shown in Figure 6(a). The corresponding single-stage equivalent is given in Figure 6(b).

When constructing an interpolator with a conversion factor L factorable as

$$L = R \times N \quad (4)$$

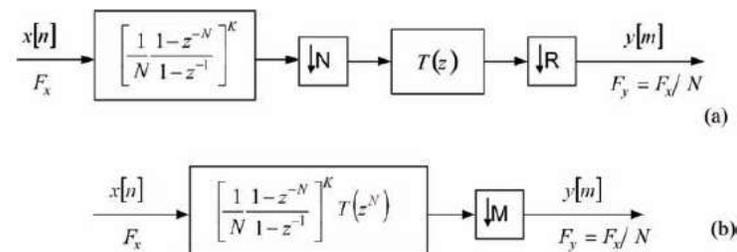


Figure 6: Two-stage decimator composed of a CIC filter and an FIR filter:
 (a) Cascade implementation.
 (b) Single-stage equivalent

It might be beneficial to implement the last stage as a CIC interpolator. The first stage is usually implemented as an FIR filter. Figure 7(a) depicts the two-stage interpolator consisting of the cascade of a factor of R FIR interpolator and a factor of N CIC interpolator. The corresponding single-stage equivalent is shown in Figure 7(b)

In the two-stage solutions of Figures 6 and 7, the role of CIC decimator (interpolator) is to convert the sampling rate by

the large conversion factor N , whereas the FIR filter $T(z)$ provides the desired transition band of the overall decimator (interpolator) and compensates the pass-band characteristic of the CIC filter.

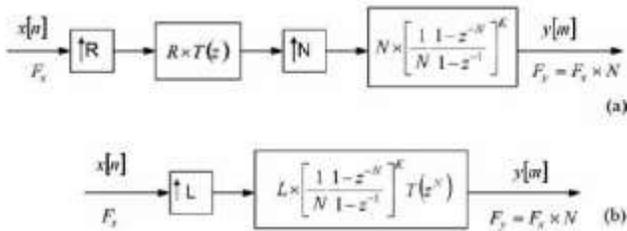


Figure 7: Two-stage interpolator composed of an FIR filter in the first stage, and the CIC filter in the second stage:
(a) Cascade implementation.
(b) Single-stage equivalent [3]

Filter $T(z^N)$ ensures the desired transition band, compensates the pass-band droop of the comb filter of the first stage. The CIC filter $H(z)$ has its two nulls just in the undesired pass-bands of the periodic filter $T(z^N)$ that ensure the requested stop-band attenuation of the target two-stage decimator[3]. Finally, we compute the frequency response of the overall two-stage decimation filter,

$$H_1(z) = H(z) \cdot T(z^N) \quad (5)$$

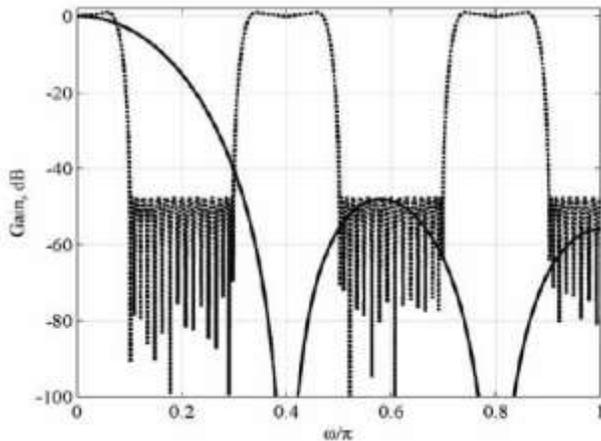


Figure 8: Gain responses of the CIC filter $H(z)$ (solid line), and that of periodic FIR filter $T(z^5)$ (dashed line).

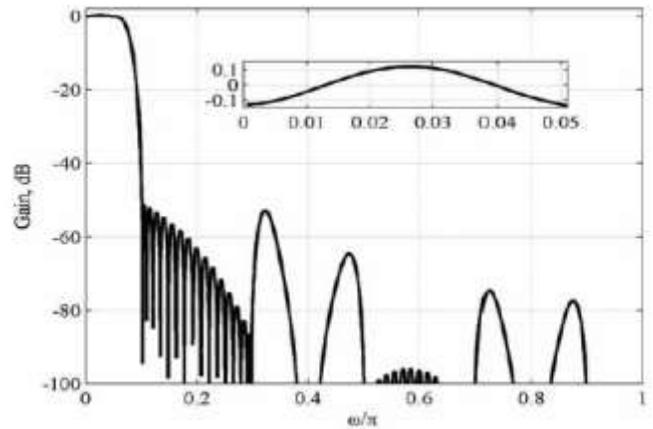


Figure 9: Gain responses of the two-stage decimator implemented as a factor of 5 and a factor of 2.

F. Filters with non integer Decimation factor: Farrow Filters

When the decimation factor $1/R$ or the interpolation factor R is an integral value, then the conversion of sampling rate can be performed conveniently with the aid of fixed digital filters [8]. In case of a scenario where the factors are irrational, it will be impossible to use fixed digital filters directly. Moreover, if R is considered as the ratio of two relatively large prime integers, then, in the case of the conventional poly-phase implementation, it is quiet essential that the orders of the required filter become very large [8]. It means that a large number of coefficients need to be stored in coefficient memory. In sample rate conversion by non-integer factor, it is required to determine the values between existing samples. In this case, it is very convenient to use interpolation filters. Among them, polynomial-based filters are generally assumed to provide an efficient implementation form directly in digital domain. Such filters witness an effective implementation through Farrow structure or its higher version [8]-[13]. The main advantage of the Farrow structure is based on the presence of fixed finite-impulse response (FIR) filters as one of its ingredients. Thus eventually there is only one changeable parameter being the so-called fractional interval μ . Besides this, the control of μ is easier during the operation than in the corresponding coefficient memory implementations [6], and the concept of arithmetic preciseness; not the memory size limits the resolution of μ . These characteristics of the Farrow structure make it a very attractive structure to be implemented using a VLSI circuit or a signal processor [6].

Consider the diagram shown in Figure 10. The dashed line separates the filter into a section running at the input signal's sampling-rate and a section running at the output sampling rate [5]. Note that the output is re-labeled to be $y[m]$ rather than $y[n]$. This is due to different input and output rates. Notably, the fractional delay now denoted β_m will now change at every instant an output sample occurs.

II. DESIGN EXAMPLES

This section illustrates the properties of the proposed filters by means of design examples.

A. Comparison of CIC filters with and without compensation:

The specifications for DDC for WiMAX are as follows:

- Input Sampling Frequency :91.392 MHz
- Output Sampling Frequency:11.424 MHz
- Pass-band Edge :4.75 MHz
- Pass-band Ripple :0.14 dB
- Stop-band Attenuation :92 dB

1) Simulation results of CIC filter is as follows:

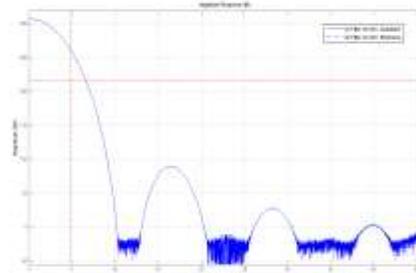


Figure 11: Magnitude Response of DDC for WiMAX using CIC Filters

2) Simulation results of CIC filter with compensation is as follows:

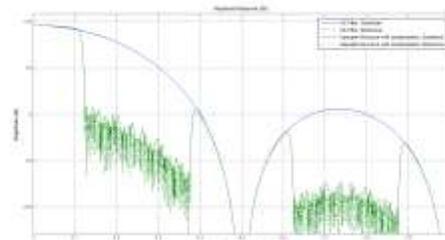


Figure 12(a): Magnitude Response of DDC for WiMAX using CIC Filters using compensation

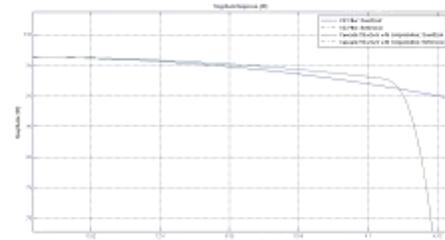


Figure 12(b): Magnitude Response of DDC for WiMAX using CIC Filters with Compensation

Both of the above filters are implemented in Altera's Stratix II FPGA family with device number EP2S15F484C3.

TABLE 1: Comparison of implementation cost and speed analysis of CIC filter and its cascaded structure with compensation:

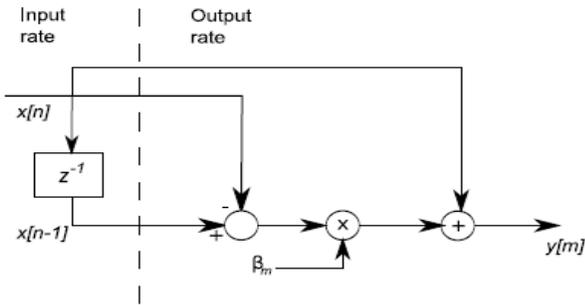


Figure 10: Multi-rate Farrow Filter

Now consider a case where the sampling rate is increased by a factor of 2. Since for every input there are two outputs, the value held in the delay register will be used twice. The first time an input is used, β_m will take on the value 0.5 and the output will be computed as

$$y[m] = 0.5(x[n-1] - x[n]) + x[n] = 0.5x[n-1] + 0.5x[n]$$

Before the input sample changes, one more output sample will be computed. β_m will take the value 0 and the output will simply be

$$y[m+1] = x[n] \quad (7)$$

Subsequently, the input sample will change; β_m will be once again set to 0.5 and so forth.

In summary, when increasing the sampling rate by a factor of two, β_m will cycle between the values {0.5, 0} twice as fast as the input, producing an output each time it changes.

In the general case, it is simply a matter of determining which values β must take. The formula is simply

$$\beta_m = \left(\frac{mf_s}{f_s'} \right) \text{ mod } 1 \quad (8)$$

Where f_s is the input sampling rate and f_s' is the output sampling rate.

In order to perform non integer SRC one can use Farrow structure or its modifications directly. However, in many cases, it becomes more efficient to use cascaded structures engineered by the modification of the Farrow structure and fixed FIR, or multistage FIR filter [12], [13]. The main advantage of using the cascaded structures instead of the direct modification of the Farrow structure lies in the fact that in case of joint optimization of the two building blocks the computational complexity to generate practically the same filtering performance is dramatically reduced. This is because of the following reasons. First, the implementation of a fixed linear phase FIR interpolator is not very costly, compared to the Farrow structure. Second, most importantly, the requirements for implementing the modification of the Farrow structure become significantly milder. This is mainly because of that the FIR filter takes care of pass-band and stop-band shaping, where the Farrow-based structure should only take care of attenuating images of FIR filter.

PROPERTY	CIC Filter	Cascaded CIC Filter with Compensation
Logic Utilization	29%	63%
t_{su}	7.425 ns	6.654 ns
t_{cq}	7.379 ns	6.619 ns
Clock Frequency	203.54 MHz	21.91 MHz

From the above simulation and implementation results, it can be concluded that the CIC filter are efficient for low-cost implementations. Due to absence of multipliers, they also have faster response. But the pass-band droop present in CIC filters restricts the scope of applications. With compensation technique, the response of CIC filter in pass-band is improved, but at the cost of extra hardware.

B. Comparison of FIR and Farrow Sample Rate Conversions:

Consider a design example to change the sampling rate by a factor of 1.536 (192/125). The design to change the sample rate by an arbitrary factor is considered. The results obtained for the simulations are as follows:

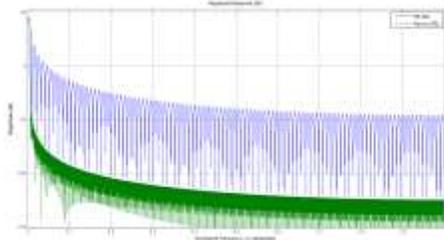


Figure 13(a): Response of FIR SRC (blue) and Farrow SRC (green) for the factor of 1.536 changes in sample rates.

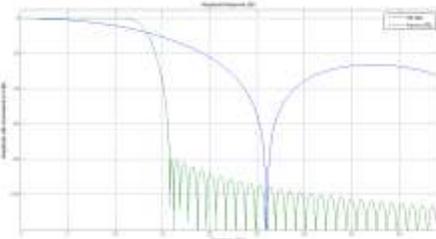


Figure 13(b): Response of FIR SRC (blue) and Farrow SRC (green)

From figure 13, it is clear that the response of farrow structure is better than the normal filter. Also, the efficiency of farrow filters is more as compared to other one. Both of these filters are also implemented efficiently in Altera's Stratix II FPGA family with device number EP2S15F484C3.

The MODELSIM simulation results of above designed filters are shown in figure 14-17.

III. CONCLUSION

Sample rate conversion (SRC) is the process of changing the sampling rate of a data stream from a specific sampling

rate (e.g. the input/output hardware rate) to another sampling rate (e.g. the application rate). Though the implementation of Signal Processing systems on ASICs provide better optimized devices, but the cost of such devices are rising. Also, the specification alteration requires the complete re-design of the system. With the recent advances in FPGA technology, the more complex devices providing high-speed as required in DSP applications are available. Also, the FPGA has advantage of reconfiguration which provides an upper hand over ASIC devices. The filter implementation in FPGA, utilizing the dedicated hardware resources can effectively achieve application-specific integrated circuit (ASIC)-like performance while reducing development time cost and risks.

In this paper, CIC filter and cascaded CIC filter for compensation is implemented in Altera's Stratix II FPGA for the specifications of Digital-Down Converter of WiMAX. Though the CIC filter have upper hand on the basis of cost of implementation and speed, but the response of compensated CIC filter proves to be more reliable.

Apart from CIC filters, Farrow filters are also implemented on FPGA for SRC. Result shows that the Farrow filters are more efficient and have better response than FIR filters for arbitrary SRC Design.

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