Very Low Power Viterbi Decoder Employing Minimum Transition and Exchangeless Algorithms for Multimedia Mobile Communication

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***Abstract*— A very low power consumption viterbi decoder has been developed by low supply voltage and 0.15 µm CMOS process technology. Significant power reduction can be achieved by modifying the design and implementation of viterbi decoder using conventional techniques traceback and Register Exchange to Hybrid Register Exchange Method (HREM), Minimum Transition Register Exchange Method (MTREM), Minimum Transition Hybrid Register Exchange Method (MTHREM), Register exchangeless Method and Hybrid Register exchangeless Method. By employing the above said schemes such as, HREM, MTREM, MTHREM, Register exchangeless Method and Hybrid Register exchangeless Method; the viterbi decoder achieves a drastic reduction in power consumption below 100 µW at a supply voltage of 1.62 V when the data rate of 5 Mb/s and the bit error rate is less than 10^{-3}. This excellent performance has been paved the way to employing the strong forward error correction and low power consumption portable terminals for personnel communication, mobile multimedia communication and digital audio broadcasting. Implementation insight and general conclusions can particularly benefit from this approach are given.**

Keywords- Hybrid register exchange method; minimum transition register exchange method; minimum transition hybrid register exchange method; register exchangeless method; hybrid register exchangeless method.

I. INTRODUCTION

The convolutional encoding and viterbi decoding schemes [1] is used by many mobile communication, satellite communication or broadcasting systems [2, 3]. Because the scheme shows powerful forward error correction performance and the great progress in CMOS technology makes it possible to realize the high speed, low power encoders/decoders [4]. A viterbi decoder [5, 6] is an important target for power reduction in many low power communication devices such as cellular phones, where it consumes almost one third power [7]. Higher memory order codes can achieve superior performance without requiring additional channel bandwidth. However, to counteract the exponential dependence of viterbi decoder complexity on memory order in low power designs, good power reduction methods are needed. Continuous efforts by defining various power reduction algorithms or approach such as Hybrid Register Exchange Method (HREM), Minimum Transition Register Exchange Method (MTREM), Minimum Transition Hybrid Register Exchange Method (MTHREM), Register exchangeless Method, and Hybrid Register exchangeless Methods are given by the author in [8, 9, 10, and 11].

As in the case of memory designs today, the significant power reduction potential lies in the dynamically varying a viterbi decoder implementation according to real time changes in system characteristics. The goal of the approach proposed in this paper is to reduce power consumption while decoding convolutional codes in a system where acceptable bit error rate varies in real time. There are following main contributions of this paper.

1) A system dependent, low power approach for decoding convolutional codes namely Hybrid Register Exchange Method (HREM), Minimum Transition Register Exchange Method (MTREM), Minimum Transition Hybrid Register Exchange Method (MTHREM), Register exchangeless Method and Hybrid Register exchangeless Methods are demonstrated.
2) Variation in the potential of these approaches as system characteristic maximum acceptable bit error rate (MABER) varies is studied.
3) Comparisons of power reduction potential of above mentioned approaches are demonstrated.

II. BACKGROUND

For the purpose of this work, a viterbi decoder implementation that employs register exchange can be described in terms of memory ‘m’, registers used for storing the survivor memory and free distance of convolutional code. A Minimum transition and Exchangeless algorithm decoders can be described with one additional characteristic, threshold. Viterbi decoding with Register Exchange method is performed by using the bits received to generate the path that represents likely transitions made by the convolutional encoder state machine over time and transfer the likely data bits to every state registers at every time. The convolutional encoder memory order determines the height or number of states per stage of the trellis, which represents the number of paths stored at any time by the viterbi decoder.

The proposed approaches, referred to as minimum transition and exchangeless decoding algorithms reduces power consumption by adopting threshold employing register exchange method to real time system changes; such as the maximum acceptable bit error rate (MABER). These approaches greatly impart power consumption because threshold controls the average number of paths stored per trellis stage and number of registers required to store these paths. The number of operations performed by the decoder, especially the memory access and ultimately the switching activity is highly dependent on the average number of path stored and the number of states (register used for storing path).Maintaining the Integrity of the Specifications.

III. SYTEM ARCHITECTURE

A Viterbi decoder and a convolutional encoder operate by finding the most likely decoding sequences for an input code symbol stream. A convolutional encoder is selected for error correction with digital mobile communication. We consider a convolutional code (3, 1, and 4) which has a code rate 'r' of 1/3 and constraint length 'K' of 5 and number of memory element 'm' is 4. The shift register taps terminate at modulo-2 adders forming generator function ($g_2 = 25$, $g_1 = 33$, $g_0 = 37$). Input bit enters the shift register by one bit at a time. The outputs of the generator functions produce an output of three symbols for each input bit, which corresponds to a code rate of 1/3.The implementation of the viterbi algorithm referred to as the viterbi decoder. The major blocks of a viterbi decoder are shown in Fig. 1. The role of each block is described briefly below.

- Butterfly unit: In butterfly we combine Branch Metric computation and Add Compare Select (ACS) block, which is first calculate the branch metric, then it get added to state metric to get path metric. Then compare the two path metrics and select the lower path metric path which is a survivor for that state.
- Survivor path storage: it stores the survivor path metric for further computation and decision regarding whether it is lesser than threshold or not.
- Output decoding block: it produces decoded bits.
- Control unit: it provides the synchronization and initiates the control signals to all blocks.

IV. DECODING METHODS

There are two standard methods used in viterbi decoder to decode the data bits; namely register exchange and traceback methods. We employ the register exchange method and modified it for power reduction.

A. Register Exchange Method

In Register Exchange Method, a register is assigned to each state which contains information bits for the survivor path throughout the trellis. Total number of states and the corresponding register requires are 2^m. The register keeps the partially decoded output sequence along the path. The register exchange method eliminates the need to traceback since the register of final state which is same as initial state S_0 contains the decoded output. This approach results in complex hardware

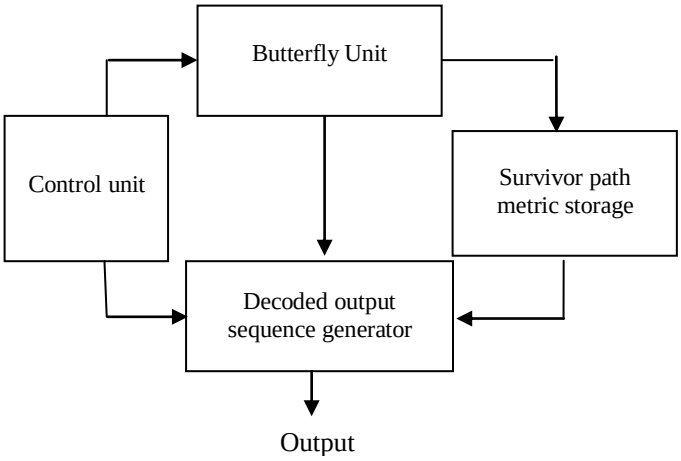

Figure 1. Block diagram of viterbi decoder

and high switching activity due to the need to copy the content of all the registers from state to state at every time. So the power consumption of viterbi decoder using REM is very high.

B. Hybrid Register Exchange Method

In this method, register exchange and traceback methods are combined and therefore the names Hybrid register exchange method [8]; which reduces the switching activity and power. Here, we are using a property of trellis is that, for m cycles the data bits will be the corresponding present state bits irrespective of the initial state from where the data gets transferred? To find the initial state we have to traceback through an 'm' cycles by observing the survivor memory, and then transfer the partial decoded data from an initial state to the next state which is m cycle later (not at subsequent cycle as in REM) and the present decoded data will be the present state itself. The memory operation is not in every cycle, and it gets reduced by a factor of m. Also, the shifting of data from one register to another is reduced that is the switching activity and ultimately the power consumption will get reduce.

C. Minimum Transition Algorithms (MTREM & MTHREM)

The main drawback of register exchange method is its frequent switching activity. One of the promising solutions to reduce the switching activity is to avoid unwanted data transfer from one register to other at every time interval. The path metric at every time interval describes, how much bits they are differed from the transmitted sequence. In these minimum transition algorithms we use the property of free distance of the encoder. Free distance tells about the errors which can be corrected by the viterbi decoder. We setup these errors as a threshold since above which the error cannot be corrected, so there is no need for storing the survivors which has a path metric above this threshold.

At the i^{th} decoding time stage, the state who has path metric greater than the threshold are eliminated in data exchange process, where threshold is fixed value depending on free distance of encoder. Here, we require only half of the registers than simple register exchange and hybrid register exchange method i.e. $2^m/2$. This is because there are maximum $2^m/2$ states which have path metric lesser or equal to the threshold. We can avoid these states or path from data transfer, so that the

data bits transitions could not takes place and avoid undesirable switching. Also, these state registers does not contain any further data transition from these states at that time and hence further switching reduces. One of such approach is Minimum Transition Register Exchange Method (MTREM).

In Hybrid register exchange method, data transfer is taking place at m^{th} instant of time therefore switching activity is less. Here, also fix a threshold and avoid an unwanted state register and data transfer operations. At m^{th} instant of time the current data bits are the current state bits only. Here the all operations i.e. data transfer and traceback operations are placed at m^{th} instant, switching activity and power dissipation further reduce.

D. Exchangeless RE and HRE Algorithms

In register exchange method, hybrid register exchange method and minimum transition methods; each row of memory is used to trace the decoded bits, if an initial state is assumed. The bottom row register in all above methods consist an decoded data, if an initial state is S_0. Further if the initial and final states are same, then the extra rows of memory are not needed. If it is assumed that initial and final state is S_0, then only one row corresponding to S_0 is required. If we observe carefully, the path metric at every instant of time, there is only one state who has path metric less than or equal to one. Therefore if we put a threshold one then at every instant there will be only one state where data to be transferred. For the even state data is '0' and for odd state it becomes '1'. If we continue in this fashion, after the reset sequence the data at the final instant is decoded data. We can say it is a register exchangeless method. Similarly for hybrid register exchangeless method, data will be decoded after every 'm' clock cycle, where the data is only the address of that state.

The exchangeless viterbi decoder is a low power design for the viterbi decoder with the restriction of resetting the encoder register after each 'L' (survivor path length) encoded data bits and it can be used for a bit error rate of acceptable limit 10^{-5} to 0.03 for wireless applications with the assumption that there will be no consecutive errors.

V. EXPERIMENTAL RESULT

In this section, the power reduction potential of the above mentioned algorithm decoder is accessed through experimental results. For a system, with variable maximum acceptable bit error rate which is applicable when minimum error correction performance needs vary over time because of variation in the type of information being received; is experimented and corresponding power reduction is mentioned. The reason for power consumption can be significantly reduced for algorithms by reducing threshold is mainly because it affect the number of times path memory is accessed. Actually the average number of times nearly all calculations are performed per trellis stage is proportional to the average number of surviving paths per stage which is controlled by the threshold. Also the average number of memory read and write operations performed per stage is proportional to the number of state registers that are accessed during data exchange between registers.

The decoder of rate 1/3 with constraint length K of 5 has been implemented using the 0.15 µM CMOS technology which operates at a supply voltage of 1.62 V. The power dissipation of the developed decoder with various above said algorithms has been measured and plotted in fig. 2. Power dissipation of the viterbi decoder using register exchange, hybrid register exchange, minimum transition register exchange, minimum transition hybrid register exchange, register exchangeless and hybrid register exchangeless algorithms are estimated as 212.26 µW, 156.35 µW, 87.41 µW, 76.75 µW, 54.95 µW and 52.13 µW respectively at a bit error rate of 10^{-6}.

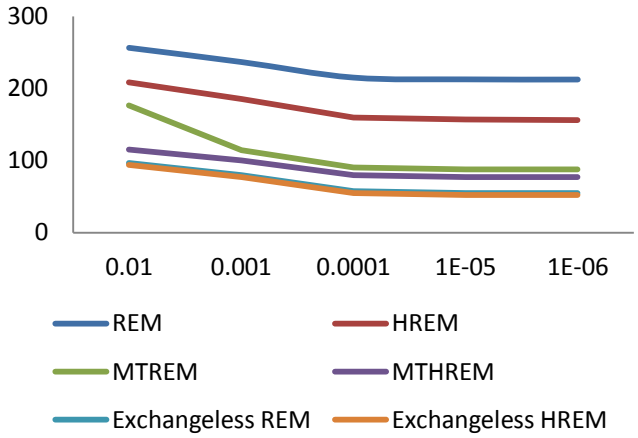

Figure 2. Power Consumption (µW) vs. BER

VI. CONCLUSION

A very low power consumption viterbi decoder is implemented with 0.15 µM technology. By applying the exchangeless hybrid register exchange method, the decoder with rate 1/3 and constraint length of 5, achieved drastic power reduction. The power consumption is reduced by almost 75% at bit error rate of 10^{-6} when the data rate is 5 Mb/s. the data rate is large enough to be implemented into the portable terminal of the audio broadcasting satellite service, mobile multimedia communication and so on.

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