

Design of A high performance low-power consumption discrete time Second order Sigma-Delta modulator used for Analog to Digital Converter

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Abstract—This paper presents the design and simulations results of a switched-capacitor discrete time Second order Sigma-Delta modulator used for a resolution of 14 bits Sigma-Delta analog to digital converter. The use of operational amplifier is necessary for low power consumption, it is designed to provide large bandwidth and moderate DC gain. With 0.35 μ m CMOS technology, the $\Sigma\Delta$ modulator achieves 86 dB dynamic range, and 85 dB signal to noise ratio (SNR) over an 80 KHz signal bandwidth with an oversampling ratio (OSR) of 88, while dissipating 9.8mW at ± 1.5 V supply voltage.

Keywords- CMOS technology; Analog-to-Digital conversion; Low power electronics; Sigma-Delta modulation; switched-capacitor circuits; transconductance operational amplifier.

I. INTRODUCTION

Analog to digital converters (ADC) with high resolution are widely used in the areas of instrumentation, measurement, telecommunications, digital signal processing, consumer electronics, etc. With the advancements in the Very Large Scale Integration (VLSI) technologies, the focus is shifted on oversampling and $\Delta\Sigma$ converters for applications requiring high precision analog-to digital conversion with narrow bandwidth [1, 2, 3, 4]. They are preferred because of their inherent relaxed sensitivity to analog circuit errors and reduced analog processing as compared to other analog-to-digital conversion techniques. These advantages come at the expense of relatively large amount of digital processing and the working of the major part of circuit at a clock rate which is much higher than the analog-to-digital conversion rate. Because of using higher clock rates and feedback loop, these converters tend to be robust in the face of analog circuit imperfections [3] and do not require trimmed components which are considered necessary in conventional high precision Nyquist rate ADCs.

For these reasons, high precision $\Delta\Sigma$ ADCs can be implemented using high density VLSI processes.

$\Sigma\Delta$ ADC is a system which consists of a $\Sigma\Delta$ modulator followed by a digital decimation filter. The $\Sigma\Delta$ modulator over-samples the input signal i-e performs sampling at a rate much higher than the nyquist rate. The ratio of this rate to the Nyquist rate is called over-sampling ratio (OSR).

After over-sampling, it typically performs very coarse analog-to-digital conversion at the resulting narrow-band signal. By using coarse digital-to-analog conversion and feedback, the quantization error introduced by the coarse quantizer is spectrally shaped i-e the major portion of the noise power is shifted outside the signal band. This process is called quantization noise shaping. The digital decimation filter removes the out-of-band portion of the quantization error and brings back the output rate to Nyquist rate.

The paper is organized as follows. Section II presents a review of $\Sigma\Delta$ modulator with theoretical analysis. Section III presents the described structure of the second order $\Delta\Sigma$ modulator with simulations results. In section IV, all main parameters of the proposed modulator are indicated with a full comparison of the most popular designs in which the performance of each modulator is cited in table IV. Conclusion is drawn in Section V.

II. REVIEW OF SIGMA-DELTA MODULATOR

Signal-to-noise ratio (SNR) and Dynamic range (DR) are two most important specifications commonly used to characterize the performance of over-sampling sigma-delta ADCs [5]. The system design begins with the calculation of the dynamic range. According to the design theory, the DR of a sigma-delta modulator can be gotten by following formula.

$$DR(dB) = 10 \log_{10} \left[\frac{3}{2} \frac{(2L+1)}{\Pi^{2L}} OSR^{2L+1} (2^B - 1)^2 \right] \quad (1)$$

The theoretical DR is a function of the modulator order L, oversampling ratio OSR, and the numbers of bits in the quantizer B.

The expression (1) reveals that an additional bit in the internal quantizer can roughly obtain a 6-dB improvement of DR. This improvement is independent of the OSR, while the improvement obtained with increasing the order L is dependent on it. The DR of a theoretical L th-order Sigma-Delta converter increases with OSR in (L + 1/2) bits/octave. This is shown in Figure 1, where the DR is plotted as a function of the oversampling ratio and the modulator order, in case of a single-bit internal quantizer.

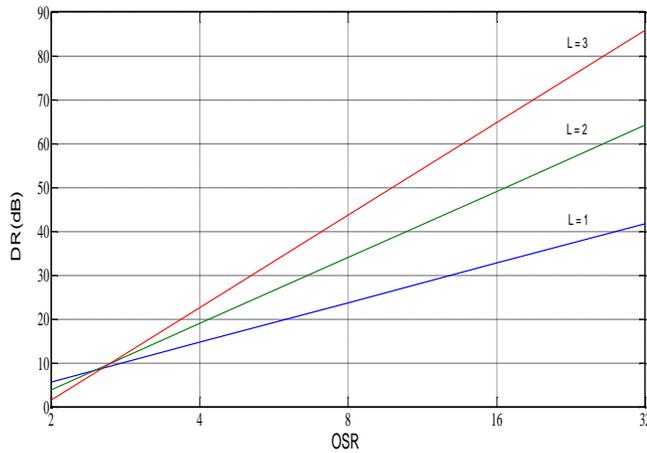


Figure 1. DR Vs OSR of Lth-order theoretical $\Sigma\Delta$ Modulators

The SNR of a converter is the ratio of the input signal power to the noise power measured at the output of the converter. The maximum SNR that a converter can achieve is called peak signal-to-noise-ratio (SNR_p). The noise here should include the quantization and circuit noise. The SNRP of the L-th order Sigma-Delta modulator can be calculated as:

$$SNR_p = \frac{3\Pi}{2} (2^B - 1)^2 (2L + 1) \left(\frac{OSR}{\Pi}\right)^{2L+1} \quad (2)$$

The SNR of the $\Sigma\Delta$ ADC can be increased by $(2L + 1)$ 3dB, or $L + 0,5$ bits by doubling the oversampling ratio, where L denotes the order of the loop filter. It is tempting to raise the oversampling ratio to increase the SNR of the Sigma-Delta modulator. However, it is restricted by the speed limit of the circuit and the power consumption.

In practice, for the same performance, it is preferred to lower the oversampling ratio. Another driving force is the ever increasing bandwidth requirement, which also needs to lower the oversampling ratio.

For high bandwidth converters, the oversampling ratio should be kept as low as possible. A lot of efforts have been made at the system level to lower the oversampling ratio and maintain the same performance.

Starting from the desired 14-bit of resolution, the Sigma-Delta ADC was designed. The DR is computed as follows:

$$DR^2 = 3 (2^{2 \times N - 1}) \quad (3)$$

$$DR^2 = 3 (2^{2 \times 14 - 1}) \quad (4)$$

Where N represents number of bits, hence DR (dB) is equal to 86.04dB. For computing the OSR for first, second and third order devices, a small MATLAB script was developed using the following equation:

$$OSR = \left(\frac{2}{3} \frac{DR^2 \Pi^{2L}}{2L + 1} \right)^{\frac{1}{2L + 1}} \quad (5)$$

OSR means Over Sampling Ratio which is based on the following formula:

$$OSR = \frac{F_s}{2 \times f_b} \quad (6)$$

If we choose an OSR equal to 88, F_s is the sampling frequency which is calculated to 14.08MHz, and f_b means base band frequency (80 KHz). Table I shows the results of the equation (4) for a first, second and third order.

TABLE I. OSR FOR FIRST TO THIRD MODULATOR'S ORDER

Modulator's order	OSR
1 st	960
2 nd	88
3 rd	24

For a first order modulator an OSR of 960 is needed, given a relatively high sampling frequency for the 0.35 μ m CMOS ultra-low-voltage system. For the second and third order devices, better sampling frequencies are required. Although for the third order modulator, the lowest sampling frequency is needed, this frequency implies the use of higher consumption and taking up more area. For that reason, a second order modulator was chosen for this application.

N is the effective number of bits of $\Delta\Sigma$ converter which is given by [6]:

$$N = \frac{1}{2} \log_2 \left[(2B - 1)^2 (2L + 1) OSR^{2L+1} / (\pi)^{2L} \right] \quad (7)$$

Where B represents number of bits of the quantization circuitry ($B = 1$).

In this case, OSR is equal to 88, F_s is the sampling frequency which is calculated to 14.08MHz. We obtained an effective number of bits equal to 14 bits which verify the two last results in equations (1) and (3).

III. PROPOSED SECOND ORDER SIGMA -DELTA MODULATOR

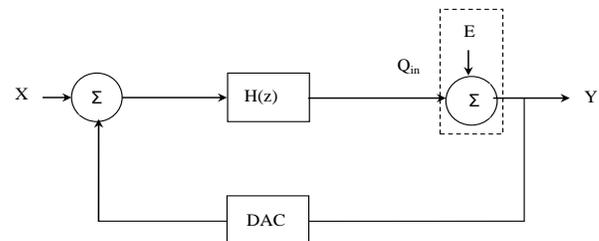


Figure 2. Linear model of conventional first order $\Sigma\Delta$ Modulator

As shown in figure 2, first-order $\Sigma\Delta$ modulator has the advantages of being simple, robust and stable. Despite these good points, its overall performance in terms of resolution and idle-tone generation is inadequate for most applications. Second-order $\Sigma\Delta$ modulator overcomes these disadvantages at the expense of increased circuit complexity and reduced signal range. According to figure 2, the modulator can be considered as a two-input $[E(z)$ and $X(z)]$, one-output $[Y(z)]$ linear system. The output signal is expressed as:

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \quad (8)$$

Where $STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer functions, which are given by:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \quad (9)$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \quad (10)$$

By using superposition principle, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z).X(z) + NTF(z).E(z) \quad (11)$$

If we choose $STF(z)$ equal to Z^{-1} and $NTF(z)$ equal to $1-Z^{-1}$ we obtain:

$$STF(z) = z^{-2} \quad (12)$$

$$NTF(z) = (1 - z^{-1})^2 \quad (13)$$

In this case, the output signal for the ideal linear model can be written as:

$$Y(z) = X(z).z^{-2} + E(z).(1 - z^{-1})^2 \quad (14)$$

To achieve the objective cited above, All main parameters of the described modulator are summed up in Table II.

TABLE II. DESIGNED MODULATOR PARAMETERS

Parameters	Value
Order of modulator	2
Sampling Frequency (clock)	14.08 MHz
Signal Band width	80 KHz
Over sample Ratio(OSR)	88
Resolution	14 bits

The functional diagram of the second order modulator simulated using Simulink in MATLAB is shown in Figure 3. The single bit DAC is replaced by a simple wire. The input is a sinusoidal signal with 0.4 V amplitude and frequency 20 kHz. This signal is fed through two integrators and is connected to the comparator at the output.

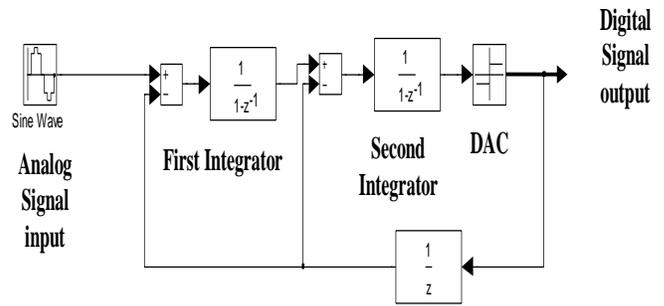


Figure 3. Block diagram of Second Order $\Sigma\Delta$ Modulator

The modulated output as seen through the scope is shown in Figure 4 with the input signal overlaid on it.

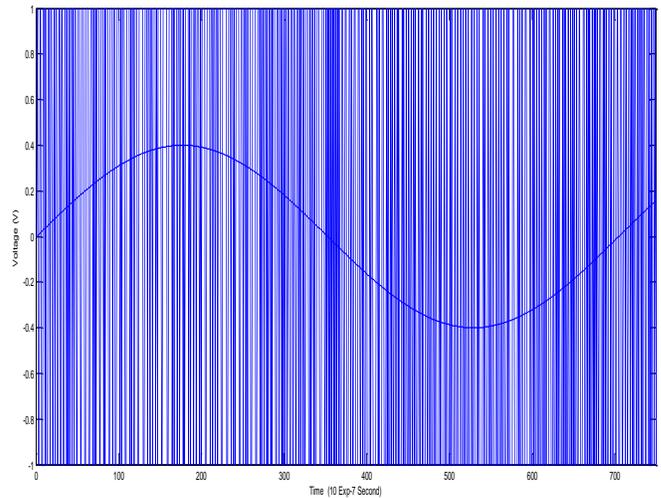


Figure 4. Pulse density output from a sigma-delta modulator for a sine wave input

A discrete Fourier Transform (DFT) of the sampled output signal is performed to calculate the SNR of the system. The logarithm of the amplitude of the signal is plotted versus the signal frequency and the SNR is found to be close to 85.17 dB as shown in Figure 5.

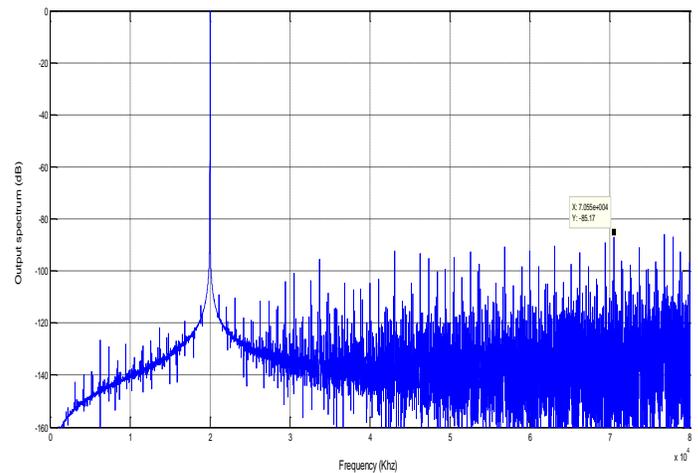


Figure 5. Frequency spectrum zoom of the modulated signal

It can be seen that second order noise shaping is taking place wherein most of the noise is pushed to the higher frequency bands as shown in figure 6. The original signal can be retrieved using a digital low pass filter.

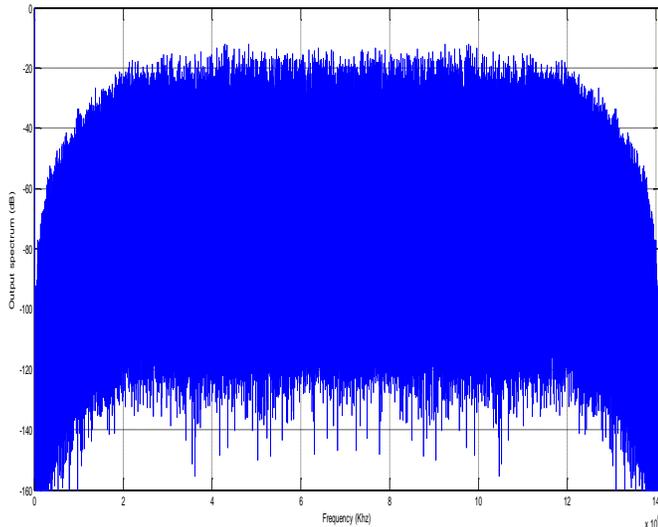


Figure 6. Frequency spectrum of the modulated signal

Figure 7 shows a block diagram of a complete Second-order $\Sigma\Delta$ modulator. It is made up of two integrators, a comparator, and digital to analog converter (DAC). These include switches Q and Q' for applying one of two reference node voltages, $+V_{ref}$ and $-V_{ref}$, depending on comparator output polarity. The two integrators are based on amplifier, and use two phase, with the respective phases denoted by ϕ_1 and ϕ_2 .

As shown in figure 7, signal sampling is completed by the first integrator connecting to the input. For this reason, the amplifier determines the whole performance of the sigma-delta modulator and needs to be carefully designed. Each integrator is made up of one operational amplifier. This operational amplifier has an adequate bandwidth and higher voltage gain. It is composed of two input transistors formed by P-channel MOSFETs M1 and M2 in order to reduce 1/f noise [7].

This stage of op-amp is also formed by N-channel MOSFETs, M3 and M4. The use of transistor M7 as a P-channel common source amplifier forms the second stage of op-amp. The polarisation block is formed by ten transistors (M5, M6, M8, M9, M10, M11, M12, M13, M14 and M15) with variable input voltage V_{in} and input resistance R_{in} .

The overall gain of the amplifier is found to be given by:

$$A_v = g_{m1}(r_{ds2} // r_{ds4}) \cdot g_{m7}(r_{ds6} // r_{ds7}) \quad (15)$$

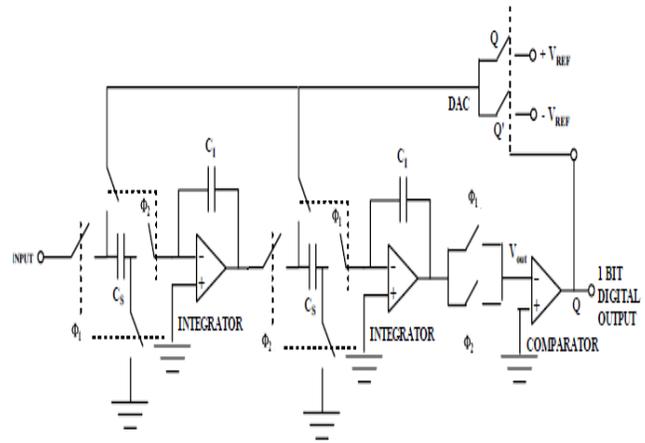


Figure 7. A complete Second-order $\Sigma\Delta$ modulator

Where g_{mi} is the transconductance and r_{dsi} is the drain to source resistance of i^{th} transistors with $i = 1, 2, 4, 6, 7$.

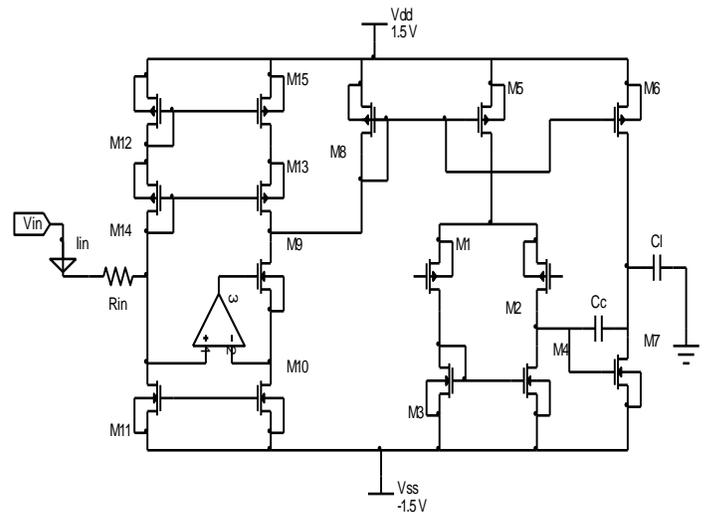


Figure 8. Miller Operational Transconductance Amplifier

Considering the appeal to moderate speed and noise of operational amplifier together with the low power consumption of the operational amplifier, Miller structure is chosen, and the structure of circuit is shown in figure 8. The system has problems of instability because the signal will pass through two-stage circuit and may bring extra pole and zero in this operational amplifier, so it requires importing frequency compensation. Simulations results using T-spice shows that output frequency response of our operational amplifier achieves a gain of 60 dB with a large gain bandwidth of 82 MHz and a phase margin of 62° to ensure more stability (figure 9).

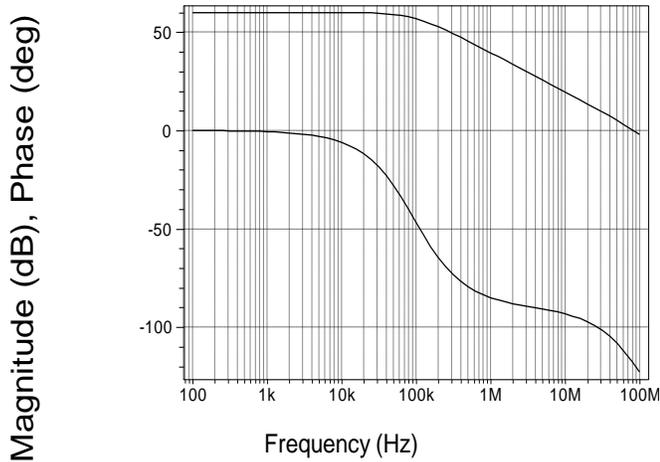


Figure 9. Frequency response of Operational Transconductance Amplifier

A. Why high performance and low power?

With the rapid development of computers and communications, a very large number of chips required to have higher performance, low power and small size. Hence analogue, mixed signals with low power and especially Sigma-Delta modulators become more and more important. Operational amplifier structure for almost all modulators circuits determine the performance of analogue structure, which largely depends on their characteristics. One of the popular op-amp is a two-stage Miller op-amp. It introduces an important concept of compensation. The object of this compensation is to maintain stability of the operational amplifier. This last is made up of three stages even though it is often referred to as a “two-stage” op-amp, ignoring the buffer stage. The first stage is composed of the input devices of the differential pair which are formed by P-channel or N-channel MOSFETs. It plays a very important role due to its differential input to single-ended output conversion and its high gain. In addition this stage of op-amp also had the current mirror circuit formed by N-channel MOSFETs. In the other hand the second stage is formed by only one transistor which serves as a P-channel common source amplifier. The current I_{bias} of the op-amp circuit goes through current mirrors formed by the rest of P-channel transistors in order to produce a low current of $10\mu A$ [17].

According to figure 10, the DC characteristic for the V-I converter for different values of resistance ($R_{out}=100\ \Omega$, $R_{out}=2.5\ K\Omega$, $R_{out}=5\ K\Omega$) is presented. In the one hand the full input voltage swing capability is evident with truly linearity. In the other hand, in order to ensure low and low consumption an input voltage V_{in} varied from $-1.1V$ to $0V$ to provide a current from $-10\mu A$ to $150\mu A$. In this case the current is equal to $10\mu A$ at input voltage V_{in} equal to $-1V$.

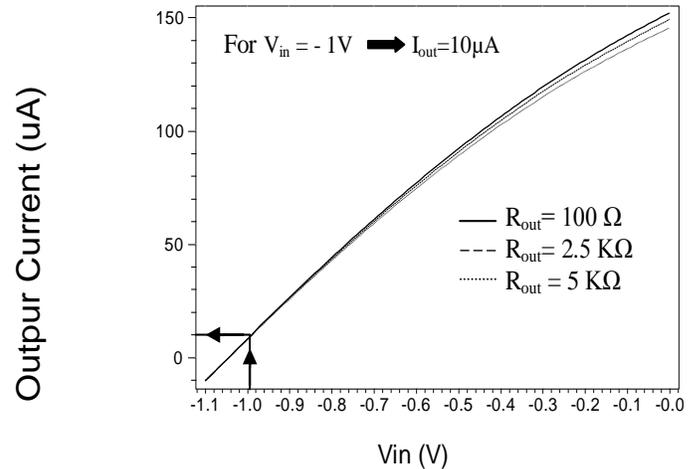


Figure 10. DC characteristics of V-I converter for different values of resistance R_{out}

From figure 8, the Miller operational amplifier is presented. Here in the polarisation circuit, an amplifier between the mirror’s input and output transistor is necessary to achieve high current copy accuracy. In the other hand we use a simple amplifier composed of only two transistors. This amplifier is proposed by K. Tanno [19] to provide low voltage, low consumption and high performance as shown in figure 11.

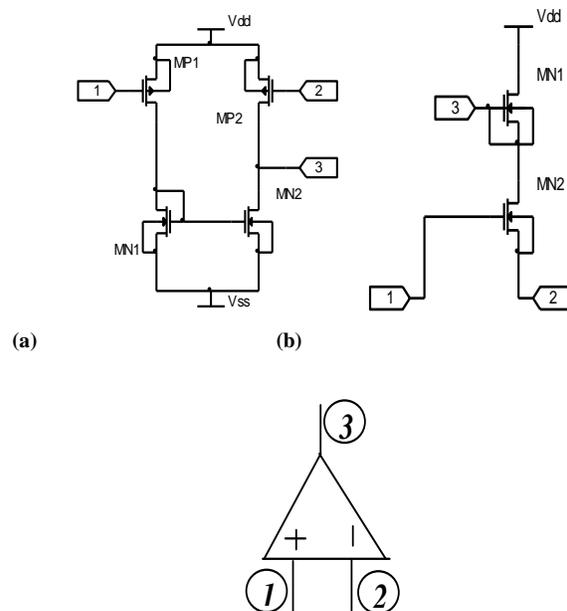


Figure 11. amplifier configuration:
(a) Simple differential amplifier structure [18]
(b) Two-transistor amplifier structure [19]

TABLE IV. COMPARISON TABLE OF MOST POPULAR DESIGNS WITH CURRENT WORK (*)

Resolution	OSR	SNR (dB)	Speed (MHz)	Power (mW)	Process (CMOS)	Signal Band width	Order	Ref. No.
14-bit	166	-	5.312	0.5	0.35µm	16 KHz	2	8
15-bit	16	96	40	44	0.25µm	1.25 MHz	2	9
10-bit	128	68	1	0.4	0.18µm	1 MHz	2	10
16-bit	64	93	3.2	5	0.35µm	25KHz	4	11
14-bit	24	85	2.2	200	0.35µm	100 KHz	6	12
11-bit	10	62.5	300	70	0.13µm	15 MHz	4	13
14-bit	96	85	53	15	0.18µm	300 KHz	2	14
16-bit	128	-	5.12	2.6	0.18µm	20 KHz	3	15
8-bit	64	49.7	1.024	6.6	0.6µm	8 KHz	1	16
14-bit*	88	85	14.08	9.8	0.35µm	80 KHz	2	This work

IV. RESULTS AND COMPARISON

The second order modulator is designed by using AMS technology 0.35µm CMOS process, the over sampling ratio is 88 with a signal band width of about 80 kHz.

All main parameters of the described modulator are summed up in Table III.

TABLE III. T DESIGNED MODULATOR PARAMETERS

Parameters	Value
Technology	AMS 0.35 µm
Order of modulator	2
Sampling Frequency (clock)	14.08 MHz
Signal Band width	80 KHz
Over sample Ratio(OSR)	88
References	±1V
Maximum Input	1 Vpp
Supply voltage	±1.5V
Resolution	14-bit
Signal to Noise Ratio (SNR)	85 dB
Dynamic range (DR)	86 dB
Quantizer resolution	1 bit
Power consumption	9.8 mW

The current state of the art in the design of $\Sigma\Delta$ modulator is limited by the technology and the sampling speeds it is able to achieve. Here is a comparison in table IV of the most popular designs which also compares the published works with the current work. It can be seen that the current work consumes less power than most published work and achieves the resolution of 14 bits using one of the technology AMS 0.35µm CMOS process.

V. CONCLUSION

The low-power-consumption modulator is designed with switched-capacitor techniques, and the resolution reaches 14 bits in AMS 0.35 µm CMOS process. Compared to other $\Sigma\Delta$ modulators, the second order single $\Sigma\Delta$ modulator has many advantages on performance, stability, area and system specification requirements, especially the power consumption.

When the power supply is ±1.5 V, the power consumption is only 9.8 mW.

In the future work, we will study and design of the different blocks constituting complete analogue to digital converter

(ADC) in transistor level, which is composed of an analog Sigma Delta modulator with a digital filter, in the other hand we will discuss about multi-bit discrete-time Sigma-Delta ADC.

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