Design and Simulation of a Low-Voltage Low-Offset Operational Amplifier

Babak Gholami
Department of Electrical Engineering
Kazeroon Branch, Islamic Azad University
Kazeroon, Iran

***Abstract*—In many applications, offset of the OP-AMPs should be canceled to high accuracy be accomplished. In this work, an asymmetrical differential input circuit with active DC offset rejection circuit was implemented to minimize the systematic offset of the amplifier. The proposed OP-AMPs show that the systematic offset voltages is less than 80 µV.**

Keywords—component; formatting; style; styling; insert

I. Introduction

The CMOS Op-Amp is an important building block of linear and switched-capacitor circuits. However, mismatch of the devices causes an offset voltage, which limits the high-precision application. Commonly, the offset sources of OP-AMPs are categorized as systematic offset and random offset. The systematic offset happens because of the channel length modulation of transistors and the value of the offset voltages are the functions of the input and output common mode voltages [1, 2, 3]. For example, in the formal OP-AMPs, the channel length modulation of transistor shows the systematic offset. However, the channel length modulation is unimportant, with no feedback, the output common mode voltage ever shows the fixed voltage level and doesn't follow the change of the input common mode voltage level. This difference between the input and output common mode level shows very small systematic offset voltages. The systematic offset can be minimized by controlling bias current of input stage to sustain the input and output common mode in same level.

The general method of offset cancelation of OP-AMPs is the feedback-capacitor circuit as shown in Fig.1 [7]. At first, as the switch 1 and 2 are turned on, the offset voltage is stored in C offset. Then the offset of V_{OUT} is omitted when the switch 1 and 2 are turned off and the switch 3 and 4 are turned on. But this circuit has some disadvantages of large capacitor, and many CMOS switches which is the source of the switching error. In this work, a continuous time asymmetrical differential input circuit with common mode feedback circuit which can minimize the offset of OP-AMPs is presented.

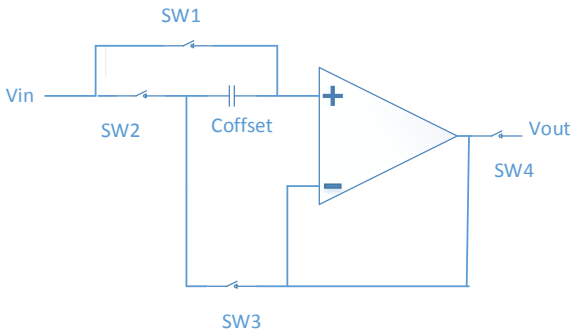

Fig. 1. Typical Offset Compensation Circuit

II. Circuit Description

The proposed OP-AMP is composed of three parts: Asymmetrical differential input stage, Common Mode Feedback (CMFB) stage and output stage. In input stage, there are cross-coupled input devices, M_1, M_2, M_3 and M_4 and tail current sources, M_5 and M_6. Input devices have asymmetrical differential structure. It means that W/L of M_1 and M_3 is larger than that of M_2 and M_4, so the transconductance (g_m) of M_1 and M_3 is larger than that of M_2 and M_4. The proposed CMFB circuit is shown in figure 3. The first stage is the combination of M_9-M_{12} and current sources M_{14}-M_{17} [10, 8].

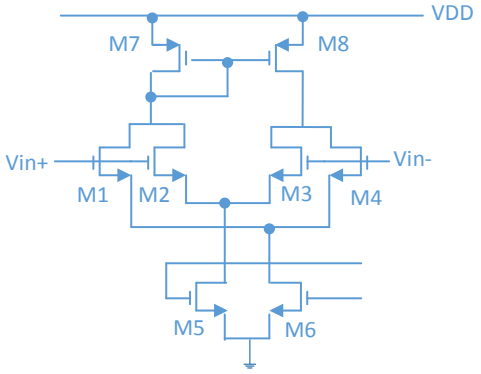

Fig. 2. Input Stage

The second stage is the combination of M_{14}-M_{19}. Long channel NMOS transistors are used for input stage to minimize the differential pair nonlinearity and to insert more input voltage swing. They also minimize the V_{bias} caused by the transistor mismatch among M_9-M_{12}. The common-mode level of the input and the output could be detected and amplified by the DC offset rejection circuit, and changed to the feedback signal for current sinks of the amplifier. This is a negative feedback network.

By adjusting the current of the current sinks, the input and the output common-mode voltage would be maintained in same level to minimize the systematic offset. The difference between input and output common-mode level will be amplified. In the proposed circuit, the sum of drain currents, I_{M5} and I_{M6} is constant. Therefore, small signal differential mode open loop voltage gain of input stage is given by:

$$A_{vd,input\text{-}stage} = -(g_{m(M3)} + g_{m(M4)}).(r_{o(M8)} \text{ II } r_{o(M3)} \text{ II } r_{o(M4)})$$

Where g_m is the transconductance and r_o is the output resistance of transistor. The total small signal open loop differential mode voltage gains are given by:

$$A_{vd} = (A_{vd,CMFB\text{-}stage}).(A_{vd,input\text{-}stage}).(A_{vd,output\text{-}stage})$$

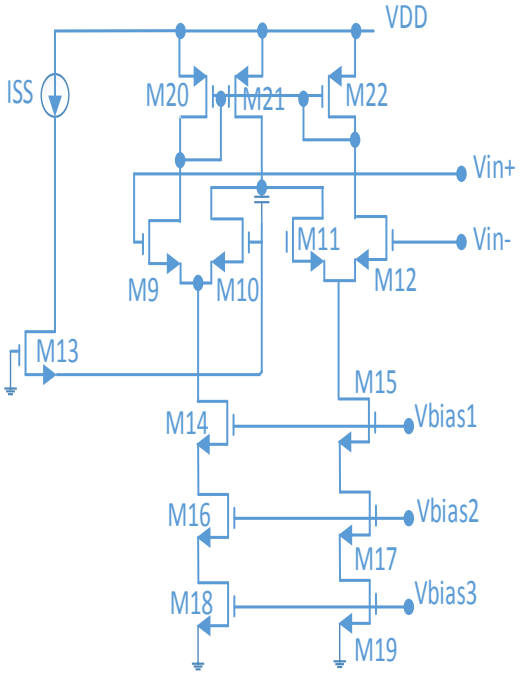

Fig. 3. DC Offset Rejection Circuit

III. Output Stage

The class-AB output stage shown in Figure 4, is composed of an output buffer. Transistor M_{23}-M_{26} form two floating current sources to provide bias current of branches, which confirm the transistor M_{33}, M_{34}, M_{35} and M_{36} work in saturation region. Their gate voltages are provided by two biasing branches respectively. The current signal I_{IN1} and I_{IN2} are subtracted through current mirror and amplified by push-pull stage [10, 2].

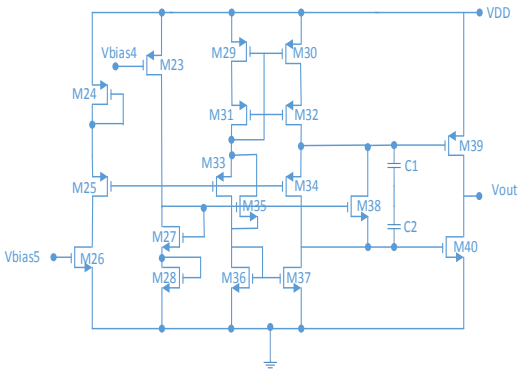

Fig. 4. Output Circuit

IV. Simulation Circuit

Figure 5 shows the AC responses of the proposed OP-AMP while driving a 2 pF load. It shows 60 dB open-loop gain, 63.5° phase margin, and 2.82 MHz unity gain bandwidth. DC sweep analysis of the amplifier connected in an inverting unity-gain configuration is shown in figure 6. The simulation results showed good following characteristic between Vin and Vout , and the offset voltage less than 80 µV by averaging.

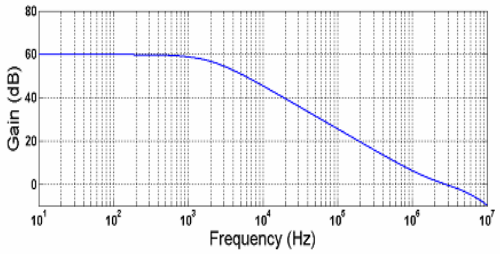

Fig. 5(a)

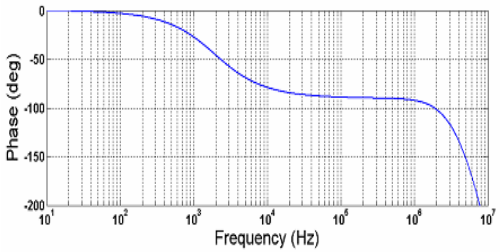

Fig. 5(b)

Fig. 5. Simulation Result of Frequency Response: (a) Magnitude, (b) Phase

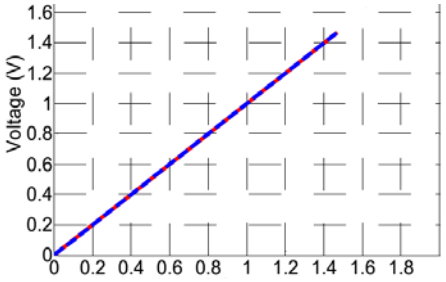

Fig. 6. The Simulation Result of the Following Characteristic

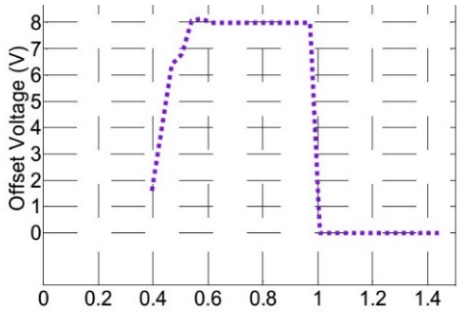

Fig. 7. The Simulation Result of the Offset Tunning Range

TABLE I. PERFORMANCE SUMMARY

CMOS Technology	0.18µm
Supply	1.5V
Gain	60dB
Phase Margin	62°
Unity Gain Bandwidth	2.73 MHz
Input Offset Voltage	80µV

V. CONCLUSION

An offset cancellation technique that uses an asymmetrical differential input circuit with active DC offset rejection circuit has been presented. Simulation results show that Op-Amp offset voltage is less than 80µV in entire operating voltage range.

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