VLSI Design of a High Performance Decimation Filter Used for Digital Filtering

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***Abstract*—With the rapid development of computers and communications, more and more chips are required to have small size, low-power and high performance. Digital filter is one of the basic building blocks used for implementation in Very Large Scale Integration (VLSI) of mixed-signal circuits. This paper presents a design of decimation filter used for digital filtering. It consists of Cascode Integrated Comb (CIC) filters, using Finite Impulse Response (FIR) filters and Infinite Impulse Response (IIR) filters structure. This architecture provides small area and low power consumption by avoiding the use of multiplication structure. This design presents the way of speeding up the route from the theoretical design with Simulink/Matlab, via behavioral simulation in fixed-point arithmetic to the implementation on either ASIC. This has been achieved by porting the netlist of the Simulink system description into the Very high speed integrated circuit Hardware Description Language (VHDL). At the first instance, the Simulink-to-VHDL converter has been designed to use structural VHDL code to describe system interconnections, allowing simple behavioral descriptions for basic blocks. A comparison of several architectures of this circuit based on different architectures of most popular filter is presented. The comparison includes: supply voltage, power consumption, area and technology. This approach consumes only 2.94 mW of power at a supply voltage of 3V. The core chip size of the filter block without bonding pads is 0.058 mm2 by using the AMS 0.35 µm CMOS technology**.

Keywords*—Digital circuit design; CIC decimation; Cascaded integrator comb filter (CIC); IIR-FIR structure

I. INTRODUCTION

Generally analog filters are cheaper, faster and have large dynamic range in both amplitude and frequency. Digital filters in comparison are vastly superior performance level that can be achieved. Quality is better than analog filters to digital filters can achieve performance unique [1]. The filtering problem is approached makes a dramatic difference [2]. With analog filters, emphasizing precision and stability, such as resistors and capacitors in electronics, controls have limitations. In comparison, digital filters are often ignored in order to better filter performance [3]. The emphasis shifts signal constraints and the processing of theoretical issues. The digital processing performance of signals and communication systems is generally limited by the quality of the input signal. The increasing use in telecommunication digital technique, like audio applications, supported the analog to digital converter use [4]. However, it proved that the traditional converters do not reach high performances on a small surface. Current research in the field of telecommunication progress exceeds the current technological limits and improves the concept of the future system performances considerably: better integration rate, low power, personal communication apparatus size reduced and the capacity of multiplying the communication number. For the signal transmission, a using of a conversion technique called modulation such as the coded pulse modulation. The basic operation in digital signal processing is filtering [5]. This operation is widely used in many electronic devices to cancel part of signal that is redundant or damages the signal. The digital filter is described by difference equation in time domain and by transfer function in frequency domain [6]. There are two basic types of digital filters: Finite impulse response (FIR) filters and infinite impulse response (IIR) filters [7]. The both types of filters have some advantages and disadvantages are summarized in Table I.

The main disadvantage of a FIR filter is high order of the filter in comparison with IIR filter with approximately the same frequency response. So the size, consumption of power and computing time of a FIR filter are higher than of IIR filter. The one of the solutions of this problem is use Interpolated FIR (IFIR) filter that significantly reduces order of the filter.

Structure of IFIR filter is described below. More details about features of FIR and IIR filters can be found in. Different structures of Digital filters are presented such as: decimation filter, comb filter, half band filter.

TABLE I. ADVANTAGES AND DISADVANTAGES OF DIGITAL FILTERS

Type of Filter	Advantages	Disadvantages
FIR	-Linear phase -Behavioral Stability -Low quantization noise -Simple implementation	High order filter
IIR	Low order filter	Stability Complicated implementation Limit cycles

The paper is organized as follows. Firstly, a presentation of decimation filter by combining FIR and IIR filters. Secondly, a description of Cascaded Integrator Comb (CIC) Filter and Half band filter are presented with behavior simulation using MATLAB. Then a presentation of synthesis process of decimator filter which shows the standard cells netlist extracted from Verilog file in order to obtain an integrated circuit design called the layout of decimation filter using Cadence. Finally, all main parameters of the described decimation filter are indicated with a full comparison of the most popular designs.

II. DECIMATION FILTER

One of the most important component which combines FIR and IIR filters is decimation filter. Its function is to remove all of the out-of-band signals and noise and to reduce the sampling rate by M, where M is the over-sampling ratio (OSR). By averaging M values of the coarsely quantized sigma-delta output, the filter gives a high resolution output at the low rate.

In the decimation [8], the frequency on the outlet side of the sample frequency F_s filter is a submultiples frequency of entry Fe. There is $F_s/F_e = 1/M$. It is then enough to filter the signal to keep only the contents of the band [0, $F_s/2$] corresponding to the new sampling rate, then not to keep that a sample on M. This filtering must be with linear phase so that a signal originally in the band [0, $F_s/2$] is not deteriorated by filtering. The filtering multi-stages reduce the complexity of the decimation filter of the converter. The first step in designing a decimation filter is to decide which types of filters will be used and where decimation will occur. It is possible to remove the undesired channels and noise with a single filter and then decimate to the output rate. The number of taps in an FIR filter is proportional to the stop band rejection and to the sampling rate divided by the transition band. The power is proportional to the number of taps and the rate at which they operate. By decimating in stages, the total number of taps in the filters is reduced and subsequent filters operate at lower sampling rates, further reducing the power consumption [8].

III. CASCADED INTEGRATED COMB (CIC) FILTER

Different structures of decimation filter are used such as: polyphase, IIR-FIR and Non-recursive structure. A polyphase structure [9], needs maximum area and minimum power consumption. Then IIR-FIR structure requires highest power consumption and minimum area on chip. In this paper we are using a hardware implementation of a multistage decimation filter using Cascaded Integrator Comb filter (CIC) shown in Fig. 1 required IIR-FIR structure. Where IIR filter works at a sampling frequency F_s and the FIR filter works at Nyquist rate F_s/M.

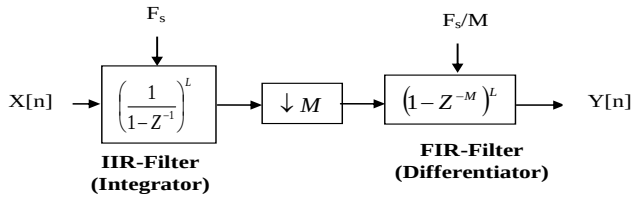

Fig. 1. Block Diagram of CIC decimation using IIR-FIR Filter Structure

Where M is the Over sampling Ratio. Moreover IIR filter can be implemented as digital integrator and FIR filter can be implemented as digital differentiator. The transfer function of the CIC filter is giving by:

$$H(z) = \left(\frac{1 - Z^{-M}}{1 - Z^{-1}} \right)^{L} \qquad (eq\ 1)$$

Where M is the oversampling ratio, L is the order of the filter. The numerator $(1\text{-}Z^{-M})^L$ represents the transfer function of a differentiator and the denominator $1/(1\text{-}Z^{-1})^L$ indicates the transfer function of an integrator. The decimation filter is made up of several stages.

A. Half band Filter Design

A Half-Band filter [10] is a special type of FIR which is very suitable for decimation by 2. It consists of two FIR filters. The decimation factor for each FIR filter is two. The first FIR filter in a chain corrects the distortion implied by the first two Sinc blocks. This is also a low-pass filter and though it has to provide a noise shaping outside the filter bandwidth. The last FIR filter is used as an element with a very high selectivity. FIR filters'design is based on a CSD (Canonical Signed Digit) representation and they have a hardwired implementation of their coefficients. For the filter coefficients design, there are number of advantages provided by CSD code over the ordinary binary representation.

First, since there are no adjacent nonzero digits in CSD code, one may expect less nonzero digits in CSD code than in the binary equivalent, which simplifies filter implementation. For the similar reason, CSD code is expected to be less sensitive to truncations which can further help in reducing add-shift operations within the multipliers while preserving initial filter properties.

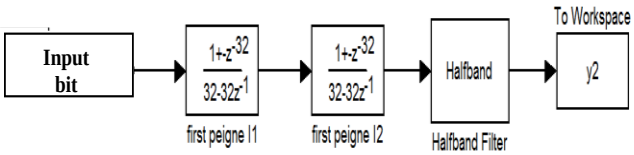

Fig. 2. MATLAB model of the Halfband Filter

CIC filter as the first stage and half-band filter as the second stage used to down sample the sampling frequency to Nyquist rate, as shown in Fig 2.

B. Design and simulations methods

a) Simulations results of the filter:

The objective is to design a decimation filter with several stages where the intermediate stages have more flexible specifications. The first stage is divided into two blocks with

decimations by 8 then by 4 to decrease the sinc filter order. The first filter is a fourth order whereas the second filter is a third order. This division is made to reduce the filter Orders and consequently their complexity. The last half-band filter has strict specifications, while the first half-band filter presents broad transition band. After simulation using MATLAB tool [11], the following curves is obtained: Fig. 3 shows the frequency response of the cascaded sinc filter.

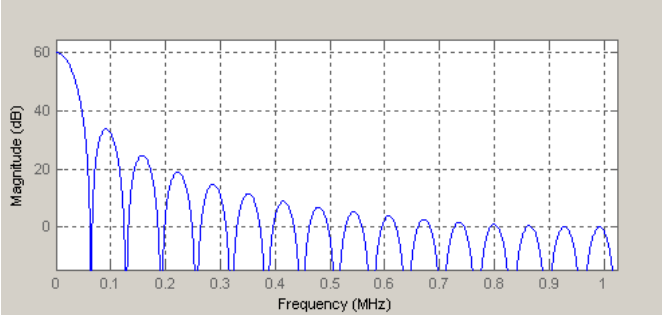

Fig. 3. Sinc filter response

Fig. 4 is the superposition of the sinc filter loss in amplitude curve and the ideal response of FIR filter.

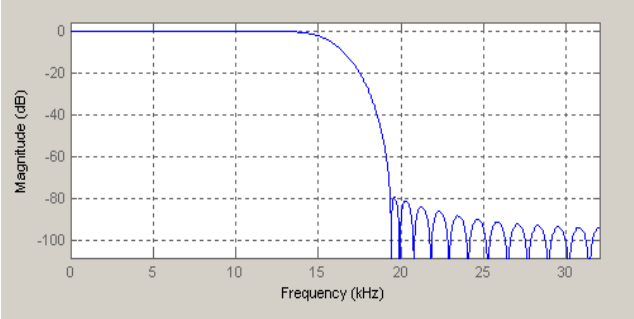

Fig. 4. Frequency response normalized and Composed after HB1

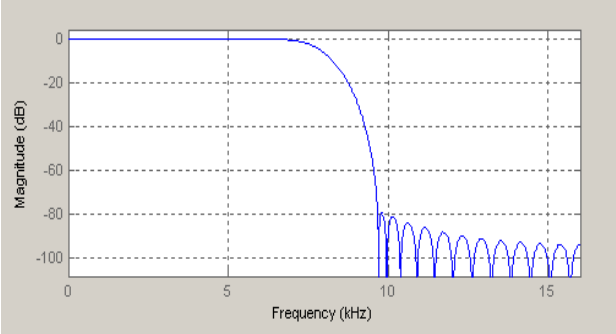

Fig. 5. Frequency response normalized and Composed after HB2

Finally, Fig. 5 presents the frequency response normalized and composed after HB2. It is the total output of the decimation chain

b) Synthesis of filter :

As shown in Fig. 6, during synthesis process, standard cells netlist was extracted and in a form of Verilog file loaded back to VHDL simulator [12]. The simulation was now performed using Cadence NCsim tool, which is a tool for logical verification, using the same test bench as before synthesis process [13]. Results of this simulation are digital samples from the filters' outputs. They are again loaded back to Matlab and processed with FFT functions. Obtained frequency this way, a design verification process was completed successfully, since the requirements are met. Using Cadence program Silicon Ensemble, floor planning, placement and routing were performed, as well as clock and reset trees generation. At the end, Verilog file is extracted and brought back to NCsim simulator where final check of the total digital part of the chip was performed.

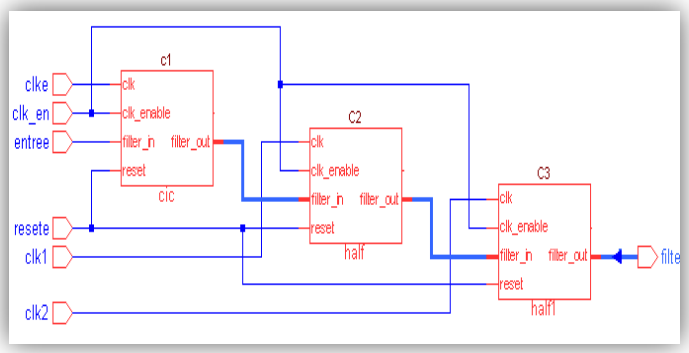

Fig. 6. Synthesis of filter

c) Layout of filter:

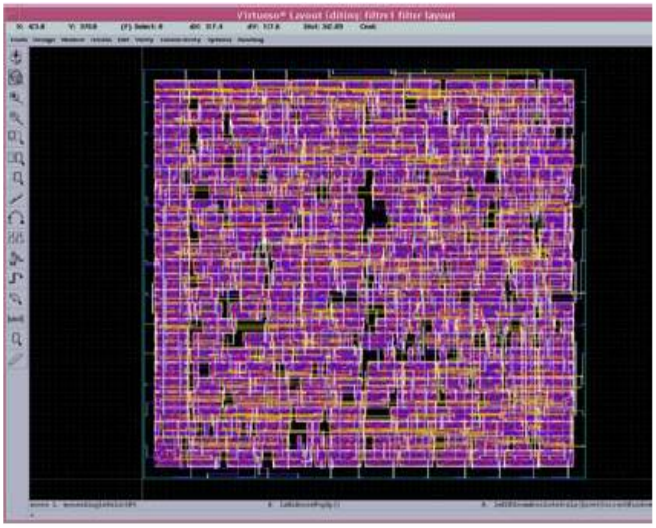

Fig. 7. Layout of decimator filter

After the step of synthesis process by extracting the cells netlist from verilog file, it is necessary to obtain an integrated circuit design. So physical design is a step in the standard design cycle which follows after the circuit design. At this step, all devices and interconnects of the design are converted into geometric representation of shapes which called integrated circuit layout, as shown in Fig 7 the layout of filter decimation obtained.

In Table II, a comparison of the most popular designs which also compares the published works with the current work. It can be seen that the current work consumes less power (2,94 mW) than most published work and also have a small

area (0,058 mm^2). In the other hand, it achieves a higher speed of 10.24 MHz.

TABLE II. COMPARISON TABLE OF MOST POPULAR FILTER BLOCKS WITH CURRENT WORK (*)

	[14]	[15]	**This Work***
Supply Voltage Vdd (V)	1.8	1.8	**3**
Power consumption (mW)	1.73	8.1	**2.94**
Area (mm^2)	-	0.2	**0.058**
Sampling Frequency (Mhz)	2.56	1	**10.24**
Technology	CMOS 0.18µm	CMOS 0.18µm	**AMS 0.35µm**

IV. CONCLUSION

Design of decimation chain made up of digital filters was successful. The multi-stages filtering reduces the complexity of the converter decimation filter. It was verified in the standard verification environment of the Cadence laboratory and is ready to use. The design is suitable for applications that require low power consumption and a small occupied silicon space. The first stage is a sinc filter carrying out decimation by 8. The second stage is also a sinc filter carrying out decimation by 4. The last two stages are half-band filters carrying out each one decimator by two. The main advantage of the design is that they can be implemented in which ever FPGA; meaning that they are not dependent on the platform. Using AMS 0.35µm CMOS Technology a Cascode Integrated Comb (CIC) filters structure consumes only 2.94 mW of power at a supply voltage of 3V. In the future work, a design of the different blocks constituting complete analogue to digital converter (ADC) by adding a block of modulator to the decimator filter will have been studying , in the other hand a Discussion about multi-bit discrete-time Sigma-Delta ADC and methodology will be described.

In the future work, we will study and design the fabrication of the proposed filter and the measurement results [16].

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