A Novel Design for XOR Gate used for Quantum-Dot Cellular Automata (QCA) to Create a Revolution in Nanotechnology Structure

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***Abstract*—Novel digital technologies always lead to high density and very low power consumption. One of these concepts is Quantum-dot Cellular Automata (QCA), which is one of the new emerging nanotechnology-based on Coulomb repulsion. This article presents three architectures of logical "XOR" gate, a novel structure of two inputs "XOR" gate, which is used as a module to implement four inputs "XOR" gate and eight inputs "XOR" gate using QCA technique. The two inputs, four inputs, and eight inputs QCA "XOR" gate architectures are built using 10, 35, and 90 Cells on 0.008 µm^2, 0.036 µm^2 and 0.114 µm^2 of areas, respectively. The proposed "XOR" gate structure provides an improvement in terms of circuit complexity, area, latency and type of cross wiring compared to other previous architectures. These proposed architectures of "XOR" gate are evaluated and simulated using the QCADesigner tool version 2.0.3.**

***Keywords*—QCA exclusive-OR; XOR gate; quantum-dot cellular automata (QCA); nanotechnology; majority gate; unique structure; QCA designer**

I. Introduction

Nowadays, the enormous increase in the number of transistors in a single chip, furthermore the reduction of the size of the transistors is an essential challenge for the design of the integrated circuits and in the VLSI technology. The problem is that in this CMOS technology, the size reduction of the transistors is limited and almost impossible beyond 10 nm since it can introduce the abnormal quantum behaviour at the nanometric scale [1]-[3].

In order to overcome this problem, and to obtain high density, the speed with low power consumption Craig Lent and al introduced a new paradigm of the architecture of calculation. This paradigm rises from a series of developments carried out in the years 1980, on the study of systems to a low emerging number of electrons of new capacities in epitaxy allowing the manufacture of gas 2D of electrons by GaAs/AlGaAs. This paradigm is quantum-dot cellular automata (QCA) technology [2], [4].

A number of advantages stem from this new technology. The first is the use of the fundamental states of elementary cells to encode information (Computing with the ground state). As in CMOS technology, maintaining the ground state requires no external energy input, and is relatively stable. This stability of the ground state can, therefore, be used as memory since once prepared, the cell remains in principle in the ground state indefinitely.

A second advantage is that the communication between adjacent cells made by Coulomb repulsion. Inside the automaton, it is not the loads, but the information itself that moves. This eliminates the need to individually control each of the internal elementary cells. This also implies that the energy is supplied to the elementary input cells only and the system, being no longer in its fundamental state, relaxes to the latter. Then the result can be read out. This operation allows a minimum of energy to perform the calculations and minimizes the connections to the cells inside the QCA. Considering that a QCA is composed of only a few input bits for several tens of internal cells, the energy efficiency of a device of this type becomes substantial. QCA technology also has the most advantages in terms of density (10^{12} devices/cm^2), frequency or speed (Range of Terahertz) and especially in terms of energy dissipation (100 W/cm^2). At this last term, several works have been carried out on the calculation of the dissipation in various operating regimes.

This QCA technology composed of an array of cells, in each one there are four several quantum dots at the corner of a square. Because of the Coulomb interaction, electrons can only occupy two "diametrically" opposed quantum dots. These two states or polarizations correspond to the electrons positioned on the diagonals square. When the electrons are in the lower corners left and higher right, polarization is defined

as P= +1 and in the diagonal opposed, it is P= -1. It is also possible to carry out planar crossings in using a turned version of 45° of a cell as shown in Fig. 1.

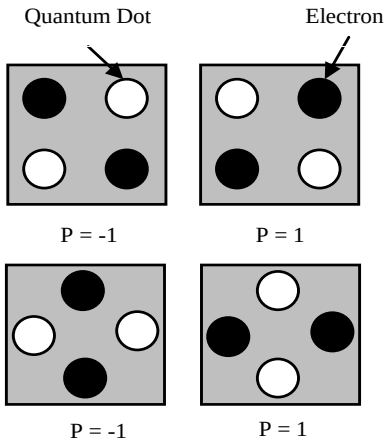


Fig. 1. Different polarizations of the quantum.

Assuming that the quantum dots at the corners of 1 to 4 (in order), we deduce that the electrons can only occupy points 1 and 3 (or 2 and 4). This is why each cell has a bistable behaviour which can facilitate its use in cellular networks on a very large scale. By taking advantage of the physical interaction between the neighbouring cells, it is then possible to implement various logical functions. The two great advantages of QCA technology is characterized by an interaction between purely Coulombic cells, and between these cells, there is no charge transport [5].

The information (logic 0 or logic 1) can propagate from input to the output of the QCA cell only by taking advantage of the force of repulsion as shown in Fig. 2.

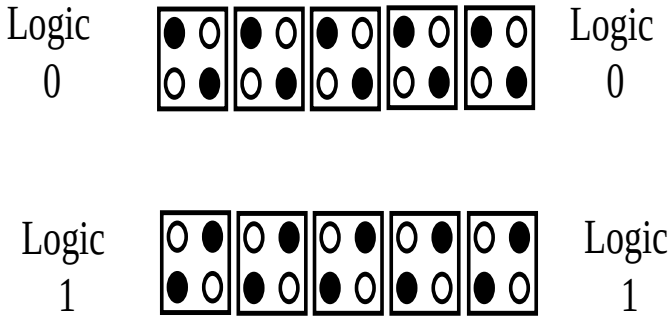


Fig. 2. Different operations of a QCA wire propagation with logic 0 and logic 1.

Thanks to these arrays of QCA technology which can be regular or irregular, the realization of various logical functions is possible. Several efforts have been devoted on a single QCA device using different approaches. Magnetic, semiconductor and molecular implants were continued, until the obtaining of the first logic functions, such as the inverter, gate shown in Fig. 3 and three-input majority voter (MV) shown in Fig. 4, which are the most important logic gate in QCA circuits.

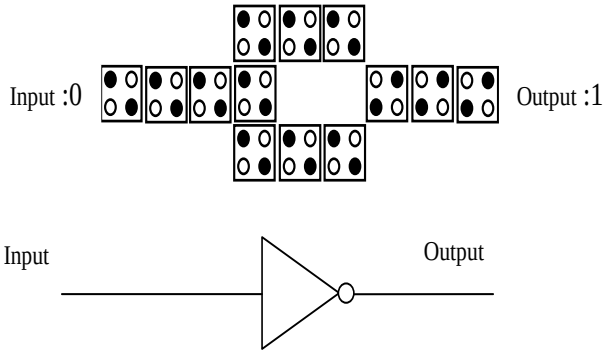


Fig. 3. QCA representation of inverter gate.

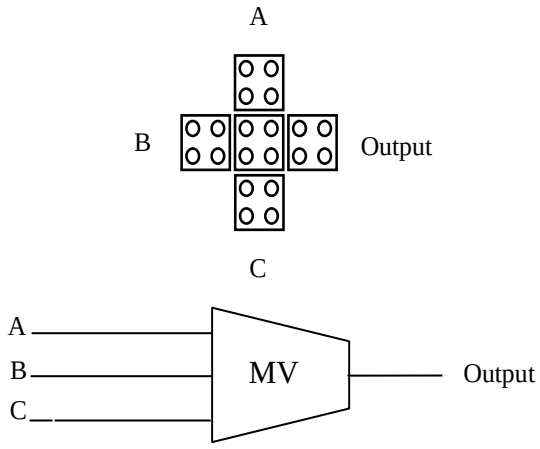


Fig. 4. QCA representation of majority voter (MV) gate.

The MV gate can behave as gate AND or gate OR logic depending on the majority logic value of its inputs. The logic function of the MV is given by this equation:

$$Output = A.B + B.C + C.A \quad (1)$$

Where, A, B, and C are the inputs of the majority voter (MV).

If one of the inputs of MV is fixed to 1 OR gate will be formed and the output will be expressed as:

$$Output = A+B \text{ when } C=1 \quad (2)$$

If one of the inputs of MV is fixed to 0 AND gate will be formed and the output will be expressed as:

$$Output = A.B \text{ when } C=0 \quad (3)$$

One of the approaches that have been proposed to make a calculation with a set of QCA cells is to apply a suitable voltage to a cell or clock [6], [7]. This involves adjusting the tunnel barriers between quantum dots in order to make the transfer of electrons from one point to another.

According to Fig. 5, each QCA cell is clocked by a clock system composed in general of four phases which are:

Switch phase: In this phase, the cells start without polarization and with low potential obstacles, while its obstacles have been raised during this phase.

1) Holding phase: In this phase the barriers are high.

2) Release phase: In this phase, the barriers are lowered.

3) Relaxation phase: In this phase, the barriers remain lowered as the previous phase. But they keep the cells in a non-polarized state.

In a clocking zone, the schema of the interdot barriers is presented in Fig. 6.

Based on the position of the potential barrier, the arrays of QCA cells in each phase have different polarizations. There are four phases; every phase has its own polarizations as shown in Table 1.

The rest of this paper is organized as follows: first, we describe the background of logical "XOR" gate or Exclusive OR gate with QCA technology. In the next, we describe different proposed 2-input, 4-input and 8-input of QCA "XOR" gate architectures with simulations results. In section IV the proposed QCA "XOR" gate architectures are evaluated and analysed. Finally, the conclusion appears in Section V.

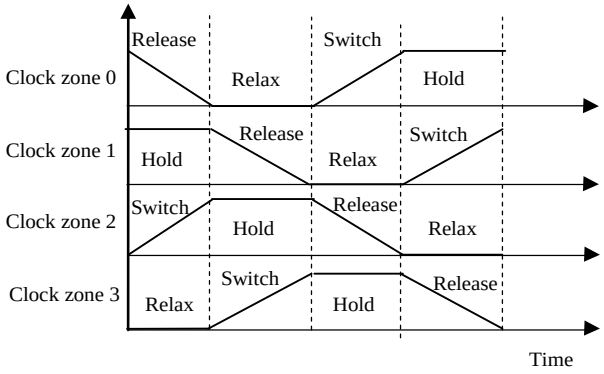


Fig. 5. Four phases of QCA clock zones.

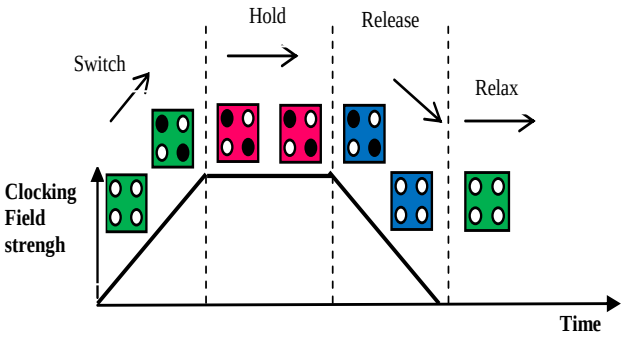


Fig. 6. Schematic of Interdot barriers in a clocking zone.

TABLE I. OPERATION OF QCA CLOCK PHASES

Clock Phase	Potential Barrier	Polarization state of the Cells
Hold	Held High	Polarized
Switch	Low to High	Polarized
Relax	Low	Unpolarized
Release	Lowered	Unpolarized

II. BACKGROUND OF LOGICAL "XOR" GATE OR EXCLUSIVE OR GATE

In this section, a description of a digital circuit called "XOR" gate is presented. It is an important digital circuit which is used in many different types of computational circuits such as Arithmetic logic circuits, Multiplexer, Full adder, Comparators and Error detection circuits.

An Exclusive "OR" gate or "XOR" gate is a digital logic gate composed of more inputs and only one output as shown in Fig. 7.

Fig. 7. General block diagram of "XOR" gate.

The output of a "XOR" gate is obtained true only if one of its inputs is true. When both of a "XOR" gate's inputs are false, or if both of its inputs are true, the output of a "XOR" gate is obtained false.

In order to design two inputs XOR gate, different architectures are proposed, but most of the researcher's designers are based on three stages: "AND" stage, "NAND" stage and "OR" stage. Where, "a" and "b" are the inputs, "Out" is the output signal as shown in Fig. 8.

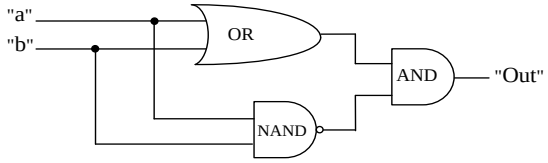
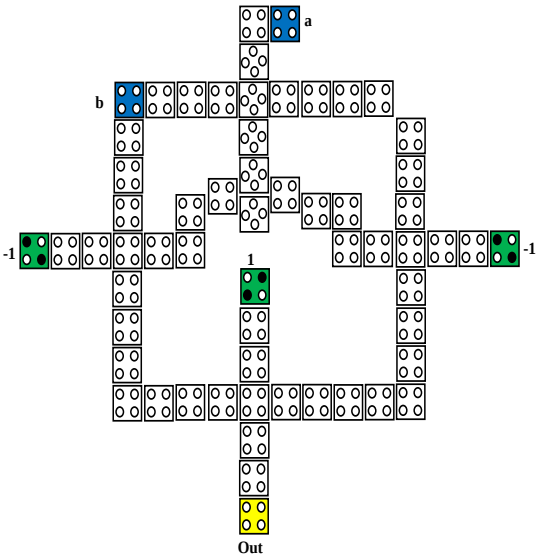


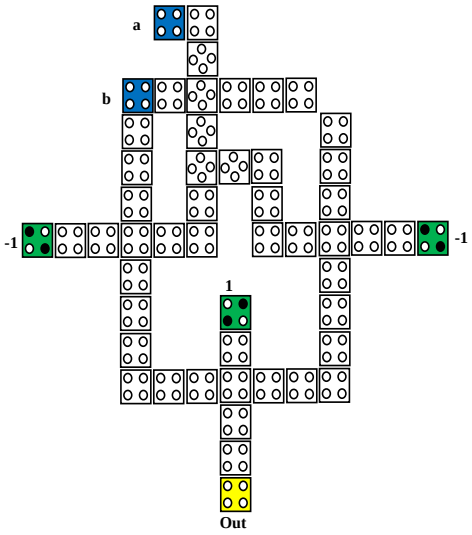
Fig. 8. Schematics of the basic architecture of "XOR" gate.

The recent previous structures of two inputs QCA "XOR" gate design are shown in Fig. 9. In [8] M.T. Niemier has designed a QCA "XOR" gate consists of 60 cells, 0.09 μm^2 area, 5 gate count and 1.5 clock zone latency as shown in Fig. 9(a). This architecture has an important number of cells and provides a large area. In order to overcome these problems, S. Hashemi et al. [9] proposed a new 2-input QCA "XOR" gate shown in with Fig. 9(b), with only 54 cells, 5 gate count, 0.08 μm^2 area and 2 clock zone latency. In order to decrease the number of cells, another structure is proposed by Chabi and al [10] which consists of 29 cells, 4 gate count, 0.03 μm^2 area and 0.75 clock zone latency as shown in Fig. 9(c). Fig. 9(d) shows another design proposed to reduce the area of the QCA "XOR" gate by G. Singh et al. [11], using two inverters, three inputs, and five inputs majority gate, with 28 cells, an area of 0.02 μm^2, 28 gate count and 0.75 clock zone latency.

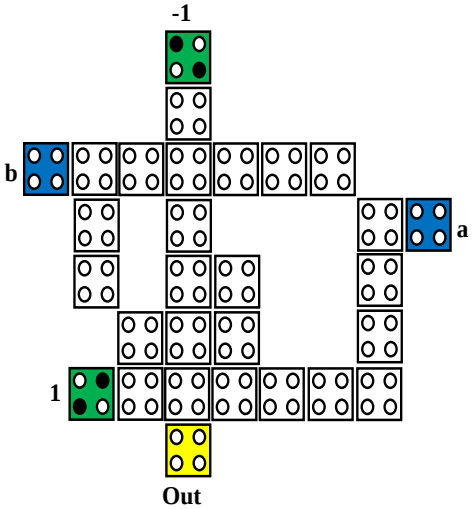
According to Fig. 9(e) and (f), A.N. Bahar et al. [12] with A. Chabi et al. [13] have reduced the number of cells until 12 cells and 14 cells, using respectively 0.0116 μm^2 and 0.01 μm^2 area, at the same clock zones latency of 0.5.



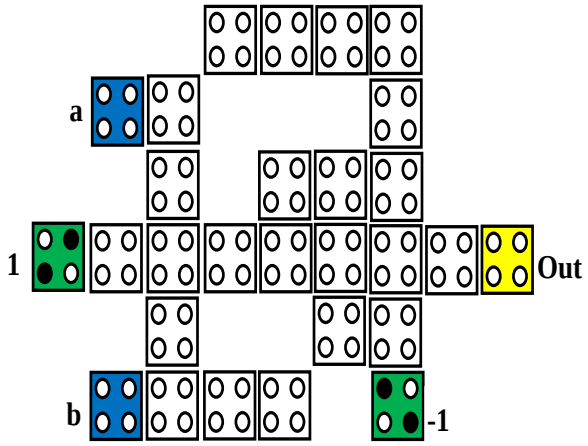
(a) [8]



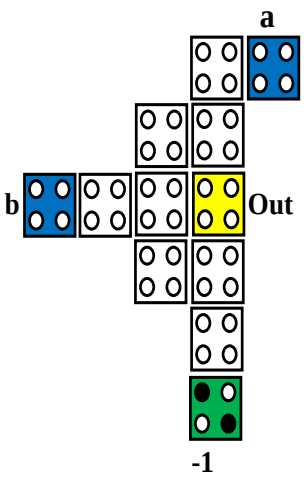
(b) [9]



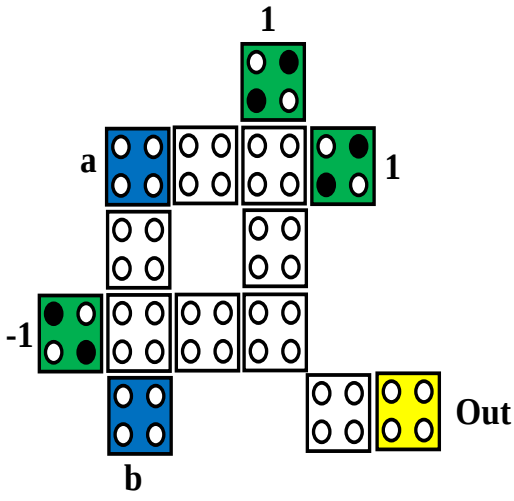
(c) [10]



(d) [11]



(e) [12]



(f) [13]

Fig. 9. The structure of two inputs "XOR" gate, (a) in [8]; (b) in [9]; (c) in [10] (d) in [11]; (e) In [12]; (f) in [13].

III. Different Architectures of Digital "XOR" Gate with QCA Implementation

A. Proposed Architecture of 2-Input Digital "XOR" Gate

The 2-input logical "XOR" gate is a hybrid circuit where its output combining between Inverter gate, "OR" gate, "AND" gate. The schematic of a simple digital "XOR" gate is presented in Fig. 10. This circuit has two inputs: "a" and "b", and one output "Out".

The truth table of this two-input "Exclusive-OR" gate is shown in Table 2.

From this table, it can be deduced that when "a" and "b" are different, the output "Out" is equal to "1", and when "a" and "b" are equal, the output "Out" is equal to "0". Hence the output "Out" of the "exclusive-OR" ("XOR") gate performs the following logic operation:

$$Out = a \oplus b = \overline{a}.b + a.\overline{b} \quad (4)$$

In this paper, a novel design of two-input "Exclusive-OR" using QCA implementation gate is proposed. It is defined by a small number of cells and high density. Then a new design of 4 inputs and 8 inputs logical "XOR" gate are designed by using the proposed architecture of 2-input digital "XOR" gate.

This novel design of two-input "XOR" gate is composed of two inputs "a", "b", and one fixed logic "0", with one output "Out". The structure and the QCA layout of the proposed QCA are shown in Fig. 11.

The simulation results of the proposed 2-input logical "XOR" gate are presented in Fig. 12. Two waveforms with different frequencies and colours are applied to the inputs (a, and b: represented by blue colour signals), the clock0 (represented by a red colour signal) and one waveform for the digital "XOR" gate outputs (Out: represented by a yellow colour signal). From Fig. 12, it can be deduced the latency of one a clock of the novel proposed "XOR" gate constituted by only 10 cells with an area of 0.008 μm^2.

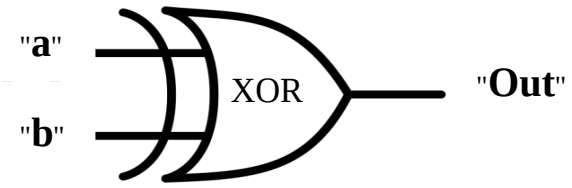


Fig. 10. Schematic of 2-input "XOR" gate.

TABLE II. Truth Table of 2-input "XOR" gate

a	*b*	*Out*
0	0	0
0	1	1
1	0	1
1	1	0

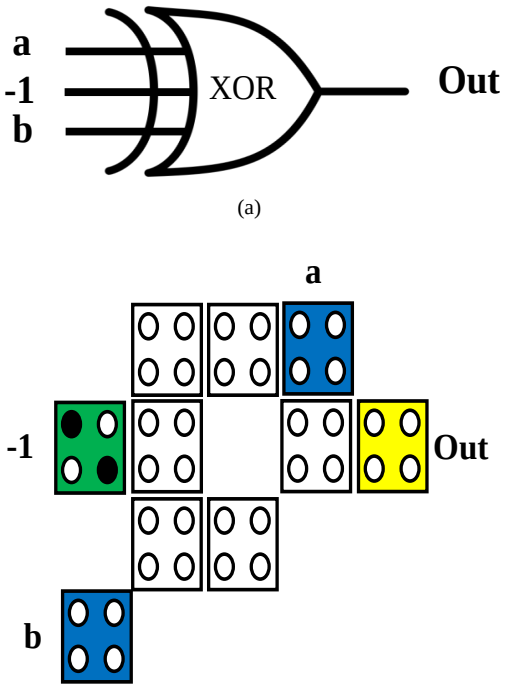


Fig. 11. The architecture of novel design "XOR" gate structure, (a)Schematic of "XOR" gate; (b) QCA layout of proposed "XOR" gate.

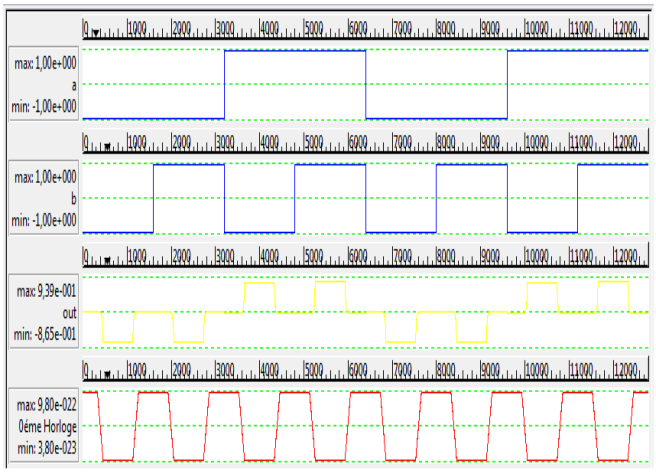


Fig. 12. The simulation result of the novel architecture of 2-input logical "XOR" gate.

B. Proposed Architecture of 4-Input Digital "XOR" Gate

The 4-input logical "XOR" gate is a combination between two elements of 2-input logical "XOR" gate. The schematic of this digital "XOR" gate is presented in Fig. 13. This circuit has four inputs: "a", "b", "c", "d", and one output "Out".

The truth table of this four-input "Exclusive-OR" gate is shown in Table 3.

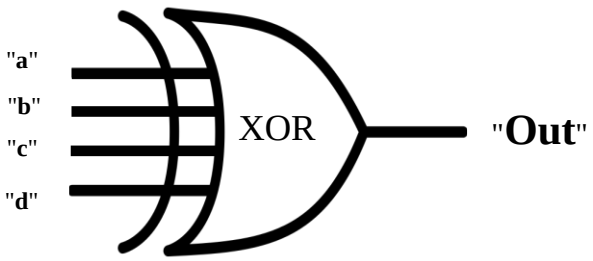


Fig. 13. Schematic of 4-input "XOR" gate.

TABLE III. TRUTH TABLE OF 4-INPUT "XOR" GATE

a	*b*	*c*	*d*	*Out*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

From this table, it can be deduced that when the number of the input "1" is impaired, the output "Out" is equal to "1". In the case of the number of the input "1" is a pair, the output "Out" is equal to "0". Hence the output "Out" of the "exclusive-OR" ("XOR") gate can determine the parity and given by the following logic operation:

$$Out = a \oplus b \oplus c \oplus d \quad (5)$$

A proposed architecture of 4-input "XOR" gate based on three blocks of 2-input "XOR" gate is composed of four inputs "a", "b", "c", "d", and three fixed logic "0", with one output "Out". The structure and the QCA layout of the proposed 4-input "XOR" gate are shown in Fig. 14.

According to Fig. 15, the simulation results of the proposed 4-input logical "XOR" gate are presented. Four waveforms with different frequencies and colors are applied to the inputs (a, b, c, and d: represented by blue color signals), the clock0 (red color signal) and one waveform for the digital 4-input "XOR" gate outputs (Out: yellow color signal). It can be interpreted that this "XOR" circuit is composed of 35 cells, the latency of six a clock, with an area of 0.036 μm^2.

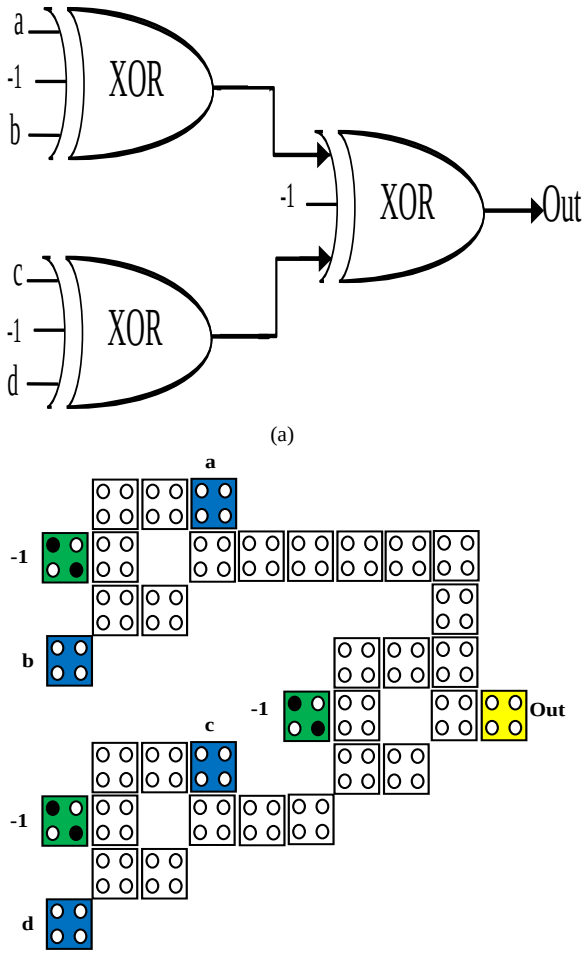


Fig. 14. The architecture of 4-input "XOR" gate, (a) Schematic; (b) QCA layout of proposed "XOR" gate.

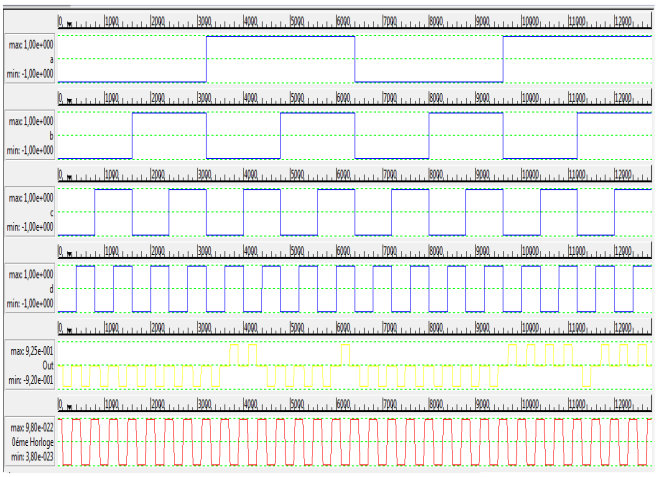


Fig. 15. The simulation result of the novel architecture of 4-input logical "XOR" gate.

C. Proposed Architecture of 8-Input Digital "XOR" Gate

The 8-input logical "XOR" gate is combined from two elements of 4-input logical "XOR" gate or four elements of 2-input logical "XOR" gate. The schematic of this 8-input "XOR" gate is constructed of eight-input: "a", "b", "c", "d", "e", "f", "g", "h", and one output "Out" as shown in Fig. 16.

The truth table of this eight-input "XOR" gate is shown in Table 4.

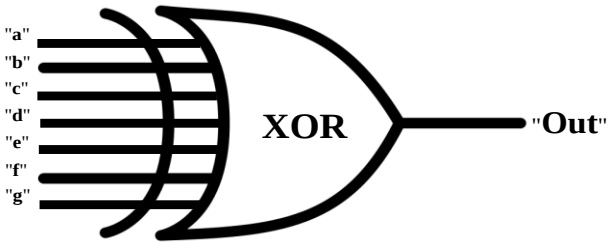


Fig. 16. Schematic of 8-input "XOR" gate.

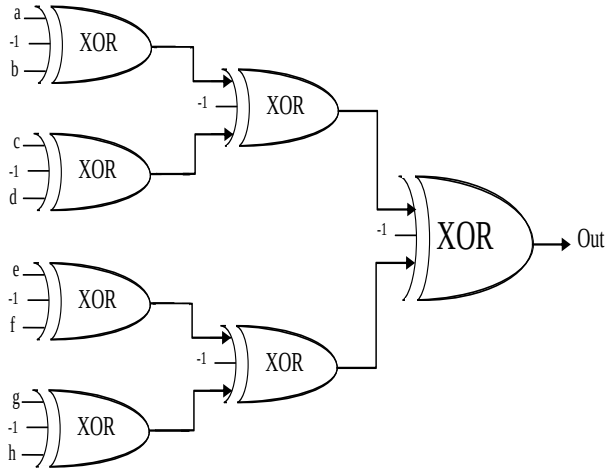
TABLE IV. TRUTH TABLE OF 8-INPUT "XOR" GATE

a	*b*	*c*	*d*	*e*	*f*	*g*	*h*	*Out*
0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	1	1	0

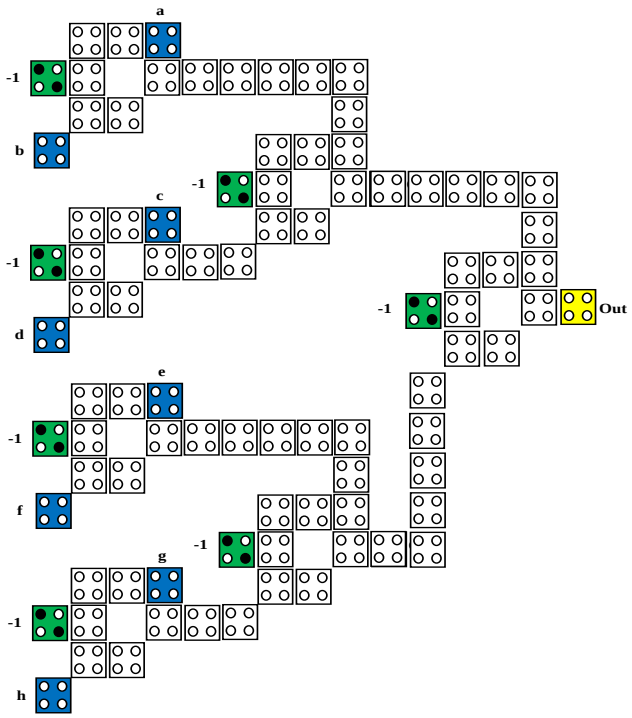
From this table, from the number of the inputs "1" is a pair or impair, the parity can be determined by the output. When "Out" = 1, the number of the inputs "1" is a pair, and when "Out" = 0, the number of the inputs "1" is impaired. Hence the output of 8-input "XOR" gate can be expressed as:

$$Out = a \oplus b \oplus c \oplus d \oplus e \oplus f \oplus g \oplus h \quad (6)$$

A proposed structure of digital 8-input "XOR" gate based on seven block of 2-input "XOR" gate is composed of eight inputs "a", "b", "c", "d", "e", "f", "g", "h", and seven fixed logic "0", with one output "Out". The architecture and the QCA layout of the proposed 8-input "XOR" gate are presented in Fig. 17.



(a)



(b)

Fig. 17. The architecture of 8-input "XOR" gate, (a) Schematic; (b) QCA layout.

The simulation results of the proposed 8-input logical "XOR" gate are presented in Fig. 18. Eight waveforms with different frequencies and colours are applied to the inputs (a, b, c, d, e, f, g, and h: represented by blue color signals), the clock0 (Clk0: red colour signal) and one waveform for the 8-input digital "XOR" gate output (Out: yellow colour signal). From Fig. 18, the latency of 96 a clock is achieved by the proposed 8-input logical "XOR" gate, which is constituted of 90 cells with an area of 0.114 μm^2.

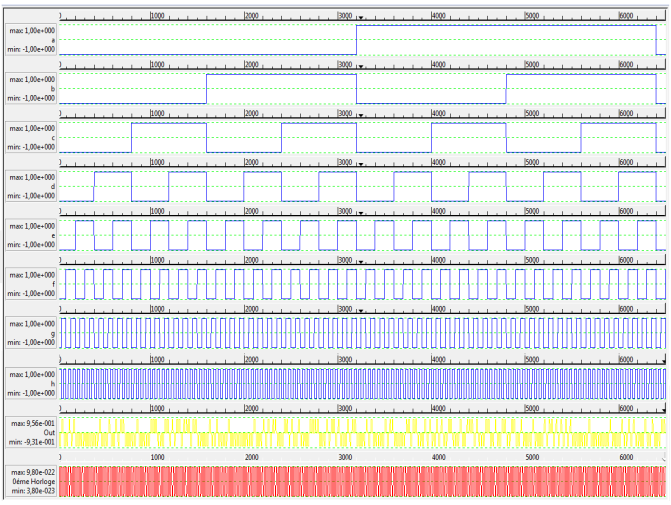


Fig. 18. The simulation result of the novel architecture of 8-input logical "XOR" gate.

IV. Analysis and Evaluation

The comparison between the proposed of 2-input digital "XOR" gate to the others architectures is given in Table 5. In this table complexity is given by the number of required cells, latency is given by the number of required clock zones, the area is given by μm^2, cell size is given by (nm) and Cross-over is either coplanar or multilayer or not required. Based on the proposed of 2-input digital "XOR" gate shown in Fig. 11, simulations results in Fig. 12 and comparative results in Table 5, the presented "XOR" gate has an improvement result in term of Complexity, and area compared with other architectures [8]-[13].

Based on the novel design of 4-input digital "XOR" implemented from 2-input digital "XOR" gate shown in Fig. 14, simulations results in Fig. 15 and comparative results in Table 6, the presented "XOR" gate has an improvement result in term of area, complexity and latency compared with other architectures [8]-[15].

Based on the novel design of 8-input digital "XOR" gate implemented from 4-input digital "XOR" gate and 2-input digital "XOR" gate shown in Fig. 17, simulations results in Fig. 18, and comparative results in Table 7, the presented 4 to 1 QCA multiplexer has an improvement result in term of area and complexity compared with other architectures [10], [11], [14], [15].

TABLE V. Comparison Results of the Presented 2-Input Digital "XOR" Gate

Structure	*Gate count*	*Area (μm^2)*	*Complexity*	*Latency (clock)*	*Cross-over type*	*Cell size (nm × nm)*
[8]	5	0.09	60	1.5	Coplanar (rotated cells)	18 × 18
[9]	5	0.08	54	1.5	Coplanar (rotated cells)	18 × 18
[10]	4	0.03	29	0.75	Not required	18 × 18
[14]	3	0.06	67	1.25	Coplanar	18 × 18
[15]	3	0.02	32	1	Not required	18 × 18
[11]	-	0.02	28	0.75	Coplanar	18 × 18
[12]	1	0.0116	12	0.5	Not required	18 × 18
[13]	-	0.01	14	0.5	Not required	18 × 18
The proposed	**-**	**0.008**	**10**	**1**	Coplanar	**18 × 18**

TABLE VI. Comparison Results of the Presented 4-Input Digital "XOR" Gate

Structure	*Gate count*	*Area (μm^2)*	*Complexity*	*Latency (clock)*	*Cross-over type*	*Cell size (nm × nm)*
[10]	12	0.19	106	1.75	Not required	18 × 18
[14]	9	0.2	188	2.25	Not required	18 × 18
[15]	9	0.11	98	2	Not required	18 × 18
[11]	-	0.1	87	1.75	Not required	18 × 18
The proposed	**-**	**0.036**	**35**	**6**	Coplanar	18 × 18

TABLE VII. Comparison results of the presented 8-input digital "XOR" gate

Structure	*Gate count*	*Area (μm^2)*	*Complexity*	*Latency (clock)*	*Cross-over type*	*Cell size (nm × nm)*
[10]	28	0.6	269	2.75	Not required	18 × 18
[14]	19	0.49	369	2.25	Not required	18 × 18
[15]	19	0.37	241	3	Not required	18 × 18
[11]	-	0.3	213	2.75	Not required	18 × 18
The proposed	-	**0.114**	**90**	**-**	**Coplanar**	**18 × 18**

V. Conclusion

This paper presented a novel and unique design of 2-input digital "XOR" gate in the QCA technology. This approach can achieve and implement 4-input and 8-input logical "XOR" gate by using the coplanar crossover technique. The simulations results are achieved by QCA Designer version 2.0.3. From these simulations, the proposed QCA multiplexer structure provides an improvement in terms of circuit complexity (10 cells), area (0.008 μm^2) and latency (1 clock) in comparison to other previous QCA multiplexer structures [8]-[13]. Different structures of 4-input and 8-input digital "XOR" gate are implemented from this 2-input digital "XOR" gate. These different digital "XOR" gates have the capability to be using in parity checking, detection and correction operations in the receiver and sender units. In addition, this architecture of "XOR" gate plays an important role in arithmetic and logical unit (ALU) of a processor. In the current proposed work, we have optimized the number of QCA cellule and reduced the wire-crossings. Further, this work may be extended to design other reversible QCA gates.

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