Design of an Error Output Feedback Digital Delta Sigma Modulator with In–Stage Dithering for Spur– Free Output Spectrum

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Abstract—Digital Delta Sigma Modulator (DDSM) is responsible for generation of spurious tones at the output of fractional n frequency synthesizer due their inherent periodicity. This results in an impure output spectrum of frequency synthesizer when they are used to generate the fractional numbers in the divider of Phase Locked Loop (PLL) based frequency synthesizer. This paper presents the design of Error – Output feedback modulator based third order Multi – stage noise Shaping (MASH) structure with lesser hardware and effective error compensation network to break the underlying periodicity of DDSM. The DDSM is also analyzed by using non-shaped, shaped and self – dithering mechanism to achieve a pure output spectrum and reduced quantization noise.

Keywords—Digital delta sigma modulator; fractional N – frequency synthesizer; phase locked loop; error feedback modulator; spur; dither; MASH; HK – MASH

I. INTRODUCTION

Phase Locked Loop based fractional N- frequency synthesizer is pillar of modern wireless communication system due to its wide range of application. They are also a favorite choice due their high frequency resolution and fast settling time. But the performance of the synthesizer is limited by the presence of spurious tones that result in an impure spectrum at its output.

The divider in the feedback path of fractional N – Frequency synthesizer as shown in Fig. 1 is based on Digital Delta Sigma Modulator (DDSM) to produce the fractional part of the divide value. The DDSMs are used to oversample and re-quantize the high resolution discrete – time input in order to produce an output with lower resolution. [1] The DDSM is a finite state machine that produces the periodic output when it is subjected to an input which is either periodic or constant input. As a result, the quantization noise in a DDSM is also periodic in nature. The output of DDSM suffers the unwanted tones due to its inherent periodicity which affect its performance. [2], [3] These tones are referred to as spurs. The position of spur in the output spectrum depends on the length of cycles produced by the DDSM. Short DDSM cycles result in strong spurs. Two classes of techniques, stochastic and deterministic are used break the length of cycles. Stochastic techniques refer to addition of random dither signal at the input while deterministic techniques deal with the structural changes in the modulator.

The recent researches have focused on developing the deterministic methods to increase the cycle length of DDSM. The extended cycle length reduces the quantization noise power in spurious [4], [5]. The techniques using error masking for reduced hardware [6] and lower power consumption using lower order DDSMs have also been proposed [7].

On the other hand, the dithering techniques are also focus of the recent researches to eliminate the spurious tones and achieve the spectral purity at the output of DDSM. [8], [9], [10].

This work inspired from idea in [10] and [11]. Authors have presented the Hybrid Key (HK) EFM structure in [11] with long cycle lengths to reduce the power of quantization noise tones. The DDSM and MASH structure is modified and efficient dithering schemes are implemented to reduce quantization noise and achieve the spectral purity.

The paper is organized as follow. The review of conventional DDSM is provided in Sec. II. In Sec. III we discuss the and HK – EFM and MASH structure based on it. Proposed Model and the simulation results with observations are discussed in Sec. IV and Sec. V simultaneously. The paper is summarized and conclusion is presented in Sec. VI.

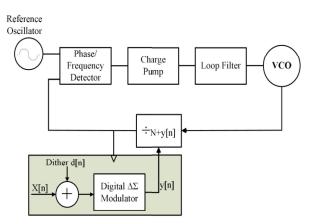


Fig. 1. PLL based Fraction N - Frequency Synthesizer.

II. CONVENTIONAL DDSM

The first order Error Feedback Modulator (EFM1) in Fig. 2 is a basic building block of MASH DDSM. It receives a digital input of N bits which passes through quantizer Q(.) with the step size of $M = 2^N$. The output is '1' when the quantizer overflows and the it is '0' when it does not overflow.

Mathematically,

$$y[n] = \begin{cases} 0, & b[n] < M \\ 1, & b[n] \ge M \end{cases}$$
(1)

The discrete output of EFM is given by

$$y[n] = \frac{1}{M}x[n] + (eq[n] + eq[n-1])$$
(2)

In Z-domain the output is represented as

$$Y(z) = \frac{1}{M} X(z) + (1 - z^{-1})E(z)$$
(3)

Where $\frac{1}{M}$ is Signal Transfer Function (STF) and

 $(1-z^{-1})$ is the Noise Transfer Function (NTF)

A MASH DDSM is formed by cascading the EFM1s and a noise cancellation network. Each EFM block has the quantization error of previous stage at its input while the carry out of each EFM1 block is fed to noise cancellation network to compensate the error at the output. A 3rd order MASH DDSM is presented in Fig. 3.

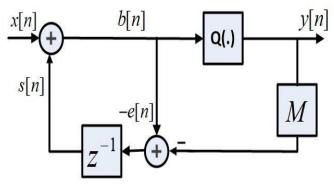
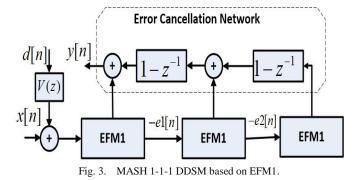


Fig. 2. First Order Error Feedback Modulator.



The output of a 3^{rd} order composed of cascaded EFM DDSM in Z – domain is as follows

$$Y(z) = \frac{1}{M} X(z) + (1 - z^{-1})^3 E(z)$$
(4)

Where NTF $(1-z^{-1})^3$ is used as noise cancellation network for a better and cleaner output.

III. HYBRID KEY – EFM

Hybrid Key Error Feedback Modulator (HK – EFM) based MASH is proved to have long cycles which are vital to reduce the number of unwanted tones at its output. The HK – MASH is based on HK – EFM1 which is different from conventional EFM in a way that it has an additional output feedback path is denoted by $az^{-1}[11]$, [12].

The output of a first order HK EFM1 is expressed as

$$Y(z) = \frac{1}{1 - \alpha z^{-1}} X(z) + \frac{(1 - z^{-1})}{1 - \alpha z^{-1}} E(z)$$
(5)

Where α is the total number of carry bits from all the stages of a MASH and is given by

$$\alpha = \frac{a}{M} \tag{6}$$

and,

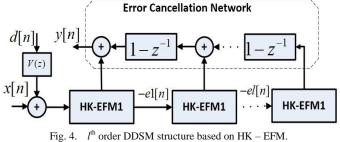
$$STF = \frac{1}{1 - \alpha z^{-1}}$$
 and $NTF = \frac{(1 - z^{-1})}{1 - \alpha z^{-1}}$ (7)

The l^{th} order HK – EFM based MASH structure developed in [11] is shown in Fig. 4. It is noteworthy that authors have considered the normalization factor and have used $(1 - z^{-1})$ in the noise cancellation network. The error of one stage is fed to the next stage as in standard MASH. The output of l^{th} order HK – EFM based MASH is given as

$$Y(z) = \frac{1}{2^{N}} \frac{1}{1 - \alpha z^{-1}} X(z) + \frac{1}{2^{N}} \frac{(1 - z^{-1})^{l}}{1 - \alpha z^{-1}} E(z)$$
(8)

with,

$$STF = \frac{1}{1 - \alpha z^{-1}}$$
 and $NTF = \frac{(1 - z^{-1})^{t}}{1 - \alpha z^{-1}}$ (9)



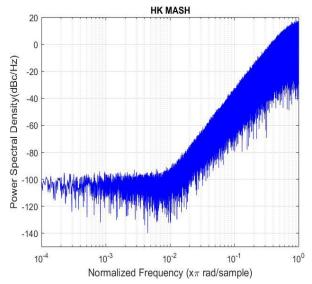


Fig. 5. PSD of MASH 1-1-1 based on EFM1 with Unshaped Dither at the Input of First Stage.

Simulated Power Spectral Density (PSD) of the system with a 15 bit quantizer setting and zero-order (or unshaped) dither applied to first stage of system is shown in Fig. 5.

IV. PROPOSED ERROR OUTPUT FEEDBACK MODULATOR AND MASH WITH MODIFIED ERROR CANCELLATION NETWORK

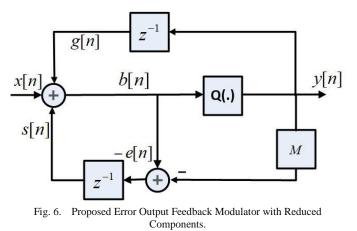
The modifications to first order HK - EFM1 and MASH structure are proposed in this work. The proposed modulator after the modification is referred to as Error Output Feedback Modulator (EOFM1) in the remainder of this paper. The proposed changes to existing HK - EFM1 and the MASH based on it are:

1) The output feedback in EOFM is without any scaling factor, instead, the actual output is fed back to the modulator. This will reduce the extra hardware required to implement the scaling factor.

2) The noise cancellation network in EOFM based MASH consists of $NTF = (1 - z^{-1})$ whereas, in previous researches, the denominator is ignored in the noise cancellation network. Possibly, because of the normalization effect in both the STF and NTF. However, in case of HKEFM, the STF is not only the scaled version of the input but is also passed through a system with transfer function $\frac{1}{1 - z^{-1}}$.

system with transfer function $\frac{1}{167}$ ($\frac{1}{167}$). 3) Finally, the techniques $\frac{1}{167}$ ($\frac{1}{167}$) (\frac

Fig. 6 shows the proposed EOFM where the output of internal signals of the modulator are as follow.



The quantization noise $e_a[n]$ is added to the output when

the input passes through an N bit quantizer with $M = 2^N$ quantization levels. Increasing the number of quantization bits can reduce quantization noise but it is not possible to eliminated entirely. The error signal e[n] is calculated by subtracting the actual signal from the quantized signal and is fed back to the input after addition of delay. The delayed output g[n] is also added with the input. Feedback signals are:

$$\boldsymbol{e}[\boldsymbol{n}] = -\boldsymbol{M}\boldsymbol{e}_{\boldsymbol{a}}[\boldsymbol{n}] \tag{10}$$

$$g[n] = y[n-1] \tag{11}$$

$$s[n] = -Me_q[n-1] \tag{12}$$

The output of the system is then

$$y[n] = \frac{1}{M} (x[n] + y[n-1]) + e_q[n] - e_q[n-1]$$
(13)

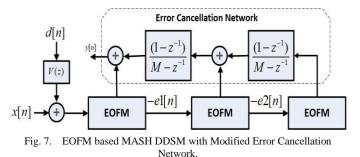
And in Z – domain as

$$Y(z) = \frac{1}{2^{N}} \frac{1}{M - z^{-1}} X(z) + \frac{1}{2^{N}} \frac{M(1 - z^{-1})}{M - z^{-1}} E(z)$$
(14)

with the following signal and Noise transfer functions

$$STF = \frac{1}{2^{N}} \frac{1}{M - z^{-1}}$$
 and $NTF = \frac{(1 - z^{-1})}{M - z^{-1}}$ (15)

A 3^{rd} order MASH DDSM is designed using EOFM. The noise cancellation network of equation no. 15 and shown in Fig. 7 is used to cancel the effect of noise from the output of each cascaded stage of the MASH structure. The error of each stage is passed to the input of next stage as in the standard MASH DDSM



The output of 3rd order MASH based on EOFM is given as

$$Y(z) = \frac{1}{2^{N}} \frac{1}{M - z^{-1}} X(z) + \frac{(1 - z^{-1})^{3}}{M - z^{-1}} E(z)$$
(16)

V. SIMULATION RESUTLS

MATLAB and Simulink have been used to simulate and analyze the performance of the proposed model. The detailed block diagram used to simulate the system is presented in Fig. 8. The system is implemented using a 15 bit quantizer with 2^{N} quantization levels.

A comparison 3^{rd} order EOFM MASH with HK MASH and standard MASH is provided in Fig. 9. PSD of output is plotted using a 15 bit quantizer and zero – order dither applied to first stage of all the systems. Other configuration for all the system are kept similar for the coherent analysis. It has been noticed that EOFM MASH does not show the performance degradation in comparison to the HK – MASH structure. However, the reduction of hardware due to decrease in each stage of the MASH is an advantage.

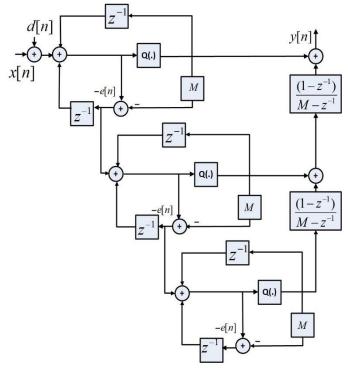


Fig. 8. Detailed Block Diagram of EOFM based MASH DDSM with Proposed Error Cancellation Network.

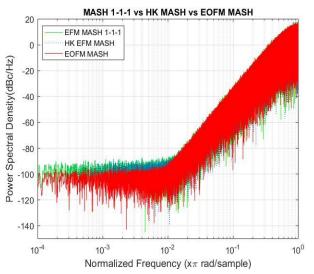


Fig. 9. Comparison of Output of PSDs EFM based MASH and HK MASH with Proposed EOFM MASH Under the Similar Conditions for all Models.

Next we have investigated the performance of our proposed DDSM by applying the efficient dithering technique that was proposed for EFM1 based MASH 1-1-1 structure where the dither is injected at the input of second and third stage together to obtain the spur free output spectrum along with the reduction of noise floor at low frequencies. We have modified the model for EOFM MASH as in Fig. 10

PSD of the model is presented in Fig. 11 which shows a reduction in noise floor in low frequencies region from -100 dBc to -170 dBc.

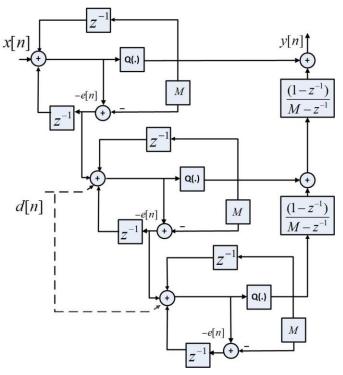


Fig. 10. Detailed Block Diagram of Proposed DDSM along with the Application of Efficient Dither Model of Gonzalez *et. al.* [13].

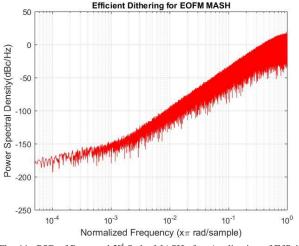


Fig. 11. PSD of Proposed 3rd Order MASH after Application of Efficient Dithering Strategy.

It is seen in the Fig. 11 that the noise floor has significantly fallen in low frequencies by applying the efficient dithering strategy vis a vis system where only the unshaped dither is applied to it and pure spectrum is also achieved. But it is further found that the obtained spectrum is similar to that when the dither is applied to the second stage only i.e. first order shaped dither. The implementation of this strategy costs the hardware overhead of applying the dither to two stages of MASH without any significant improvement in comparison to application of first order dither. Therefore, this strategy does not seem to work in case of EOFM MASH. The comparison is provided in Fig. 12.

In another investigation, the second order shaped dither is applied to proposed EOFM MASH i.e. dither is passed through second order high-pass filter $V(z) = (1 - z^{-1})^2$. The system is simulated with previous configuration settings and second order shaped dither. The PSD in Fig. 13 shows further reduction in noise floor to -250 dBc in low frequency zone with a spur free spectrujm.

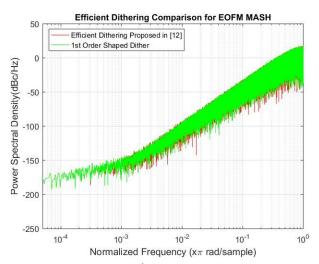


Fig. 12. PSD of Proposed 3rd Order MASH Showing the Comparison Application Of Efficient Dithering Strategy with First Order Shaped Dithering Strategy.

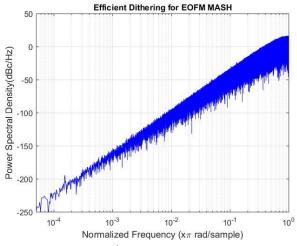


Fig. 13. PSD of Proposed 3rd Order MASH after Application of Third Order Shaped Dithering.

The comparison of the investigated dithering mechanisms is provided in Fig. 14. The graph on black color shows the output PSD when unshaped, zeroth ordered dither is applied to the proposed model. The output PSD when first order shaped dither is applied to proposed model is shown in green color while output PSD of efficient dithering strategy of Gonzalez *et. al.* is plotted in red. It is seen that both these strategies have same output performance but applying the first ordered dither can help to achieve the same performance with lesser hardware.

Finally, the graph in blue color shows the output PSD when second order shaped dither is applied. It is seen that the noise floor in lower frequencies has further fallen -250dBc in comparison to first order shaped dither where noise floor falls till -170 dBc and to unshaped dither where the noise floor stands at -170 dBc. This shows that applying the second order shaped dithering provides the best results in terms of lesser quantization noise in low frequency range and also retains the clean and spur free spectrum at the output of proposed EOFM based 3rd order MASH DDSM.

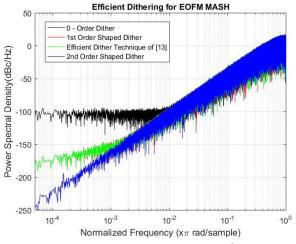


Fig. 14. Comparison of Output of PSDs of Proposed 3rd Order MASH with Different Techniques of Dither Applied to it.

VI. CONCLUSION

Digital delta sigma modulators are notorious for their spurious output due to periodic quantization noise generated due to its periodicity. The HK – MASH are helpful to reduce this quantization noise because of their long cycle length. In this paper we have presented an EOFM DDSM that has long cycle length of HK MASH with smaller hardware cost without degradation in performance.

The efficient in-stage dithering model as proposed by Gonzalez *et al.* to inject the dither at multiple points has been investigated for the proposed MASH along with the single point in–stage dither injection schemes. It has been concluded that second order shaped dithering provides better noise reduction and a pure output spectrum for EOFM based MASH in comparison to the other dithering models.

REFERENCES

- K. Hosseini, M. P. Kennedy, "Minimizing Spurious Tones in Digital Delta-Sigma Modulators" Springer Science & Business Media. 2011
- [2] V. S. Sadeghi, S. I. Saeed, S. Calnan, M. P. Kennedy, H. M. Naimi, and M. Vesterbacka, "Simulation and experimental investigation of a nonlinear mechanism for spur generation in a fractional-N frequency synthesizer" In Irish Signals and Systems Conference (ISSC 2012), 2012
- [3] S. I. Saeed, "Investigation of Mechanisms for Spur Generation in Fractional-N Frequency Synthesizers" Electronic Press, Linköping University. 2012
- [4] B. Fitzgibbon, M. P. Kennedy and F. Maloberti, "A novel implementation of dithered digital delta-sigma modulators via bussplitting," 2011 IEEE International Symposium of Circuits and Systems (ISCAS), Rio de Janeiro, 2011, pp. 1363-1366. doi: 10.1109/ISCAS.2011.5937825

- [5] Y. Donnelly, H. Mo, and M.P. Kennedy, "High-Speed Nested Cascaded MASH Digital Delta-Sigma Modulator-Based Divider Controller" In IEEE International Symposium onCircuits and Systems, 2018.
- [6] C. Y. Yao, and C. C. Hsieh, "Hardware simplification to the delta path in a MASH 111 delta–sigma modulator" IEEE Transactions on Circuits and Systems II: Express Briefs, 56(4), pp.270-274, 2009
- [7] R. LAAJIMI, and M. MASMOUDI, "Design of A high performance low-power consumption discrete time Second order Sigma-Delta modulator used for Analog to Digital Converter". International Journal of Advanced Computer Science and Applications (IJACSA), vol. 3(11), 2012.
- [8] Mo, H. and Kennedy, M.P., 2017. Masked dithering of MASH Digital delta-sigma modulators with constant inputs using multiple linear feedback shift registers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(6), pp.1390-1399.
- [9] Z. Xu, J. G. Lee, "Self-dithered digital delta-sigma modulators for fractional-N PLL. *IEICE transactions on electronics*, 94(6), 2011 pp.1065-1068.
- [10] H. Mo and M. P. Kennedy, "A high-throughput spur-free hybrid nested bus-splitting/HK-MASH digital delta-sigma modulator," 2013 European Conference on Circuit Theory and Design (ECCTD), Dresden, 2013, pp. 1-4.
- [11] B. Fitzgibbon and M. P. Kennedy, "Calculation of the cycle length in a HK-MASH DDSM with multilevel quantizers," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, Paris, 2010, pp. 245-248.
- [12] A. Telli and I. Kale, "The practical limits of MASH Delta-Sigma Modulators designed to maintain very long controllable sequence lengths for structured tone mitigation," 2009 IEEE 10th Annual Wireless and Microwave Technology Conference, Clearwater, FL, 2009, pp. 1-5.
- [13] V. R. Gonzalez-Diaz, M. A. Garcia-Andrade, G. E. Flores-Verdad and F. Maloberti, "Efficient Dithering in MASH Sigma-Delta Modulators for Fractional Frequency Synthesizers," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 9, pp. 2394-2403, Sept. 2010.