An Efficient Digital Space Vector PWM Module for 3-Φ Voltage Source Inverter (VSI) on FPGA

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***Abstract*—The realization of digital control circuitry based PWM strategies provides many advantages. It includes better prototyping, higher switching frequency, simple hardware, and flexibility by overcoming the limitations of analog control strategies. In this article, The Digital space vector-based Pulse width Modulation ((DSV-PWM) is designed. The DSV-PWM Module includes, mainly, Xdq reference frame, Sector generation, Square root, switching time generation, Carry-save adder (CSA), and PWM Generation module. These modules are designed using simple logical operations, and combinational circuits to improve the DSV-PWM performance. The DSV-PWM Module is synthesized and implemented on a cost-effective Artix-7 FPGA device. The present work utilizes a < 1% chip area, operates at 597.83 MHz of maximum frequency, and utilizes 110mW of total power on FPGA Device. The DSV-PWM module is also compared with the existing SV-PWM approach with better improvement in hardware constraints like chip area, operating frequency, and dynamic power (mW).**

***Keywords*—Digital space vector PWM; 3-phase voltage source inverter; sector generation module; switching time generation; FPGA; Verilog-HDL; Xilinx**

I. INTRODUCTION

The development of AC motor drives with present technology becomes major highlight for delivering a suitable amount of energy to the motor. This is achieved with the drastic improvements and advancement in the microprocessor, power electronics technologies and switching power converters. The amount of energy is computed by Pulse width Modulated (PWM) signals. Most of the existing analog control circuitry provides excellent dynamic response, but failed to maintain circuit complexity, circuit modification, and has few functions. The present AC motor drives adopt the processor-based or advance technology like DSP, ASIC, or FPGA based digital control strategy. The digital control strategy overcomes the existing analog control strategy limitations with more significant improvement in circuit development. The commonly used PWM approaches include the Space Vector (SV)-PWM method, Sinusoidal-PWM method, and Hysteresis-PWM method [1-2].

The 3Φ--Voltage Source Inverter (VSI) provides the Variable supply voltage to AC motor drives and is used majorly in modern industrial applications. The PWM methods are used to modulate the VSI output voltage using different controlling strategies. The SV-PWM based VSI uses many topologies, which includes, High Power 2-level VSI and Multi-level Inverter. The Multi-level inverter further classified has advanced bus Clamped-VSI, flying capacitor, or Diode Clamped-VSI and Neutral point Clamped VSI [3].

The FPGA and DSP based Controlling strategies assist different digital AC-Motor drives to control the motor. The DSP based approaches provide great features like simple circuitry, flexibility to use for many applications and software-based control strategies. But failed to maintain the bandwidth performance because of the high sampling rate used in the current control loop and PWM generation. The current control loop and PWM generation use most of the computational resources in the controller and only limited time is available to control other specified functions in the Drive. To fulfill the limitations of DSP based Controlling strategies, The FPGA /ASIC based PWM controlling strategies are used for AC motor drives. There is rapid development in FPGA, which offers faster circuit response continuously and supports parallel processing rather than sequential execution and more excellent speed control capability of 3Φ-induction motors [4-5]. The FPGA is a reprogrammable device that contains logical interconnection and logical Blocks. The logical blocks are designed with the help of logical operations, combinational, and sequential circuits. The FPGA is user friendly, avoids the high NRE cost, inflexibilities, and development cycles than the conventional ASIC approach [6-9].

In this article, an efficient Digital space vector (DSV) Pulse width Modulation (PWM) is designed and implemented on low-cost Artix-7 FPGA. It provides high performance and less resource utilization on hardware and is suitable for real-time power electronics applications. The proposed design uses simple logical operations and combinational circuits to design the DSV-PWM, which assures low power consumption, less execution time, and high reduction in chip area in FPGA and also reduces the complexity in 3 Φ-VSI.

Section II describes the existing approaches of different SV-PWM techniques from different application viewpoints and also analyzes limitations. The proposed DSV-PWM module is described in detail with the basic principle and hardware architecture in section III. Section IV discusses the simulation results and performance analysis of the DSV-PWM method and also compares with the existing SV-PWM technique with constraints improvements. Finally, the section V concludes the Overall work with improvements and suggest the future scope.

II. Related Works

This section discusses the existing approaches of different space vector (SV)-PWM techniques for different application usage. Janik et al. [10] present the SV-PWM technique without the usage of trigonometric operation to improve the hardware performance in real-time scenarios. The module investigates the multilevel converter (MLC) using independent voltage modulation. The MLC Module supports both DSP and FPGA operations on a single MLC interface unit with other supporting peripheral devices. Holtz et al. [11] present the SV-Modulator for Higher switching frequency control operation with the help of three-level Silicon-Carbide (SiC) Inverter. The design uses a two-level SV approach for switching time generation, and the Modulation module is designed based on logic decisions. The 3-Level Inverter is designed based on Circuit topologies, High-frequency PWM, Neutral point Potential (NPP) control, and 3-level Modulator. Kassas et al. [12] discuss the Look-Up Table (LUT) based SV-PWM, which is designed and implemented using simple 8-bit Microcontroller and also modeled using Simulink. The LUT used to improve the time assignment computation in 3-Φ VSI. The LUT based SV-PWM has three main modules includes PWM Timer, High, and low-priority interrupt modules for total harmonic distortion (THD) and error Calculation.

Celik et al. [13] present the real-time SV-PWM signal generation using FPGA Device. The PWM signals used to control the VSI are achieved on FPGA prototype circuit. The SV-PWM design results are verified using a time-domain simulation using Matlab Simulink. Liang et al. [14] present the SV-PWM based control algorithm on FPGA and also verify the FPGA design with a Software-based SV-PWM approach using Matlab Simulink. The SV-PWM Control algorithm includes the sector determination for any space vector, time-domain voltage space vector function generation, switching time, and conduction module. Lotfi et al. [15] discuss the SV-PWM module for voltage inverter-based AC machines. The module includes Voltage reference calculation, Sector determination, Switching time calculation, and also a series of PWM Pulses. The design uses more LUTs, consumes more chip areas and not significant for real-time applications.

The SV-PWM computations are designed for multi-level inverter by Salem et al. [16] and also for open end-winding induction machine (OEWIM) using Dual 3-level T-type converter. The operation of a 3-level dual T-Type converter is designed using vector diagrams and switching states, Sector and region identification, time interval calculation, and switching pattern modules. The design also analyzes the Voltage and current THD against different switching frequencies. Pu et al. [17] describe the Random SV-PWM technique for 3Φ- VSI on FPGA, which includes a randomization algorithm for faster and flexible realization hardware. The Random –SV-PWM has a waveform generation module, Pseudo random signal generation module, and PWM generation module. The random SV-PWM results are useful in terms of standard Line Voltage, wave filtering of Line Voltage, FFT of Line Voltage than conventional PWM approaches. Khlavi et al. [18] present the reconfigurable PWM Generator on FPGA for power electronics appliances. The module is implemented on both ASIC and FPGA, which can be configured easily with different PWM strategies. Garcia et al. [19] discuss the SV-PWM control module for 2 levels 3Φ-inverter on Matlab GUI and FPGA. The design also supports a simplified education platform for teaching SV-based PWM techniques. Suma et al. [20-21] present the FPGA controller for an Induction Motor drive and also SV-PWM based design for 3-level Inverter on non-volatile FPGA. Chinmaya et al. [22] present the analyses of different SV-PWM methods like Conventional SV-PWM, Vector space decomposition-based, vector classification based, and Common mode voltage injection-based SV-PWM approaches for dual 3Φ induction motor drive.

The proposed work overcomes the conventional SV-PWM methods by considering the performance and accuracy of the FPGA system. The present work reduces overall system cost and chip area for 3Φ-VSI on FPGA, and also present work ensures the great flexibility in FPGA for usage in real-time Power electronics applications.

III. Proposed Work

In this section, the Digital space vector-based Pulse width Modulation (DSV-PWM) designed for 3Φ-Voltage source Inverter (VSI) is explained with basic principle and its hardware architectures.

A. Basic Principle of SV-PWM

The Digital SV-PWM provides the low-current –ripple and DC-Link Voltage with better resource utilization, Lower harmonic content, Wider linear modulation index range than the conventional-SV-PWM approaches. The SV-PWM is implemented using Voltage equations in the form of the abc reference frame. This frame is converted to the d-q reference frame, and it has a horizontal (d) and vertical (q) axis. It can be determined by the Reference voltage space vector (V_{ref}), which is rotating in a circular position that constitutes a sinusoidal waveform, and it is represented in Fig. 1.

The Reference Voltage space vector estimates the combination of 8- switching forms (V_0 to V_7) in the PWM Technique. The V_1 to V_6 active (Switching) vectors are divided into 6 sectors in a hexagonal plane, and each of the sectors is arranged in 60 degrees. The V_0 and V_7 are null vectors. The V_{ref} is calculated using two null vectors and any two actives (Switching) vectors, and it is represented in Fig. 2.

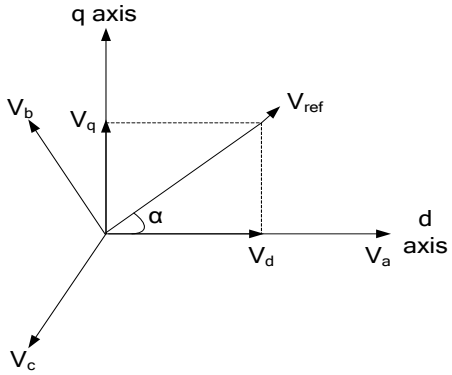

Fig. 1. Reference Voltage Space Vector.

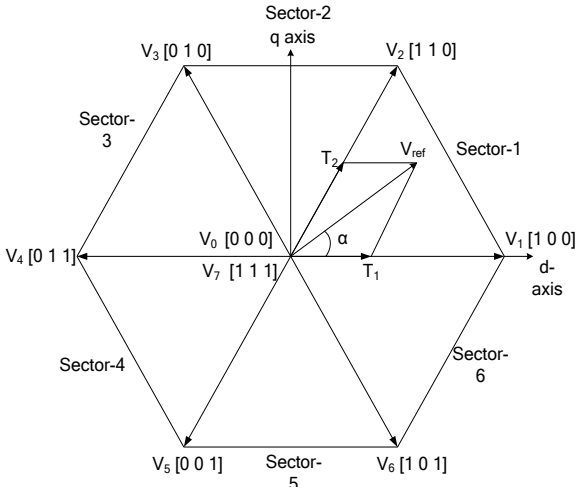

Fig. 2. Fundamental Sectors and Switching Vectors.

The three-phase voltage vector [V_a, V_b, V_c] and switching variable vector relationships are described as follows [9]:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

The reference voltage and angle are derived using eq (2) and eq (3) as follows:

$$\left|V_{ref}\right| = \sqrt{V_d{}^2 + V_q{}^2} \quad (2)$$

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) = \omega_s t = 2\pi f_s t \quad (3)$$

Where f_s is the fundamental frequency.

B. Proposed Hardware Architecture of DSV-PWM

The Hardware architecture of the DSV-PWM method is represented in Fig. 3. The DSV-PWM mainly consists of Xdq Module, Sector generation module (SGM), Switching Time Module (STM), Square root module, Carry save Adder (CSA) module, and PWM generation module. These modules are constructed using simple Logical and combinational circuits, which provide higher performance keeping the hardware constraints into consideration.

The Xdq Module is designed using equation (1), and it is simplified using intermediate vectors X_d and X_q by equation (4) and equation (5) respectively, as follows:

$$X_d = 2V_a - V_b - V_c \quad (4)$$

$$X_q = V_b - V_c \quad (5)$$

The X_{dq} Module simulation results are represented in Fig. 4. The X_{dq} Module uses simple multiplier and subtractors to generate the 8-bit X_d and X_q outputs by using the 8-bit V_a, V_b, and V_c inputs.

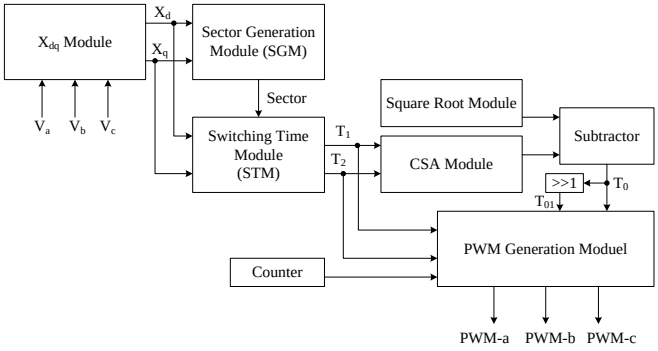

Fig. 3. Proposed Hardware Architecture of DSV-PWM Module.

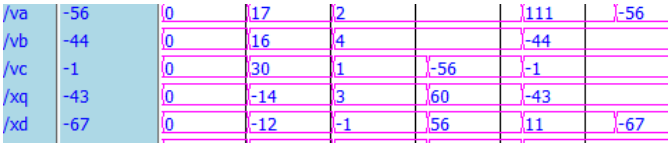

Fig. 4. Simulation Results of X_{dq} Module.

The switching variable vectors V_d and V_q are expressed by using the X_d and X_q in equation (6) as follows:

$$V_d = \frac{1}{3}\left[X_d\right] \text{ And } V_q = \frac{1}{\sqrt{3}}\left[X_q\right] \quad (6)$$

The sector generation module (SGM) is designed by using three conditions (a) sign of X_d, (b) Sign of X_q, and (c) $\left|X_d\right| = \left|X_q/2\right|$. The design uses simple combinational circuits to design these conditions. The one-bit right shift operation achieves the $X_q/2$. The sector generation is based on the following 6 rules, and it is tabulated in Table I.

The simulation results of SGM is represented in Fig. 5 using 8-bit X_d and X_q inputs along with 3-bit select line. The SGM generates the 3bit sector outputs. The SGM Hardware architecture, uses two signed Shifter modules, three multiplexers, comparators, encoder and Bit-wise logical operations (NOT and AND-gates). These modules are combinational circuits and simple to design which consume little amount of power.

TABLE I. SECTOR GENERATION

Rules	Condition	Sector
Rule-1	If (($X_d > 0$) & ($X_q > 0$) & ($X_d > X_q/2$))	1
Rule-2	If (($X_d > 0$) & ($X_q > 0$) & ($X_d < X_q/2$))	2
Rule-3	If (($X_d < 0$) & ($X_q > 0$) & ($X_d > X_q/2$))	3
Rule-4	If (($X_d < 0$) & ($X_q < 0$) & ($X_d > X_q/2$))	4
Rule-5	If (($X_d > 0$) & ($X_q < 0$) & ($X_d < X_q/2$))	5
Rule-6	If (($X_d > 0$) & ($X_q < 0$) & ($X_d > X_q/2$))	6

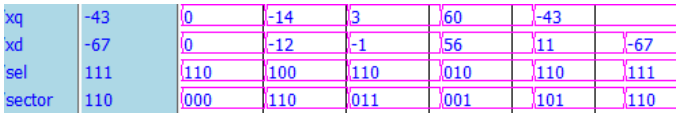

Fig. 5. Simulation Results of Sector Generation Module.

The switching time module is designed based on Table II for the generation of T_1, T_2 and T_0 using 3-bit sector generation module inputs. The T_1 and T_2 are modeled using simple right shifter, addition, and subtraction operations by using Xd and X_q.

The $\sqrt{3}$ square root module is designed using a comparator, simple multiplier, and subtractor operations. The simulation results of square root module are represented in Fig. 6.

The Switching time T_0 is generated by subtracting $\sqrt{3}$ from (T_1+T_2). The (T_1+T_2) operation is designed using an 8-bit carry-save adder (CSA). The CSA contains seven 2-bit Ripple carry adders (RCA) and three 6:3 Multiplexers. The carry-in is assumed as zero. The simulation results of 8-bit CSA are represented in Fig. 7.

The PWM module generation is designed by using the counter, Switching time and Sectors. The PWM module generation for sector -1 is tabulated in Table III. The Counter range is fixed to $2T_0 + 2T_1 + 2T_2$. The PWM pulse of a, b, and c is in the form of '0' or '1'. The T_{01} is used in Table III, which is generated using a one-bit right shifting of T_0, and it is represented in Fig. 3. Similarly, by using Sector 2-6, with different switching times, the PWM pulses are generated for a, b and c. The PWM module generation architecture uses simple shifters, adders, and multipliers. Overall, the present work uses only combinational circuits and Logical operations to construct the DSV-PWM module.

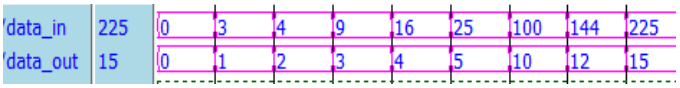

Fig. 6. Simulation Results of Square Root Module.

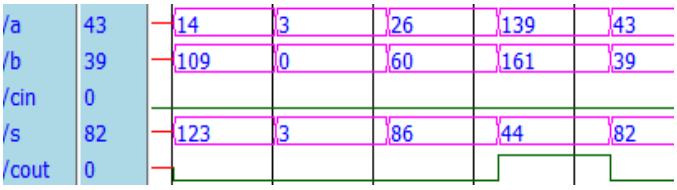

Fig. 7. Carry Save Adder (CSA) Module Simulation Results.

TABLE II. SWITCHING TIME GENERATION

Sector	T_1	T_2	T_0
1	X_d - (X_q >>1)	X_q	$\sqrt{3}$ - T_1 + T_2
2	X_d + (X_q >>1)	(X_q >>1) - X_d	$\sqrt{3}$ - T_1 + T_2
3	X_q	X_d - (X_q >>1)	$\sqrt{3}$ - T_1 + T_2
4	-X_d + (X_q >>1)	-X_q	$\sqrt{3}$ - T_1 + T_2
5	-X_d - (X_q >>1)	X_d – (X_q>>1)	$\sqrt{3}$ - T_1 + T_2
6	-X_q	X_d + (X_q >>1)	$\sqrt{3}$ - T_1 + T_2

TABLE III. PWM GENERATION FOR SECTOR-1

Sector =1			
Counter	*PWM-a*	*PWM-b*	*PWM-c*
T_{01}	1	0	0
T_{01}+ T_1	1	1	0
T_{01}+ T_1 +T_2	1	1	1
T_0 + T_1 +T_2	1	1	1
T_0 + T_1 +T_2 + T_{01}	1	1	0
T_0 + T_1 +2T_2 + T_{01}	1	0	0
T_0 +2T_1 +2T_2 + T_{01}	0	0	0

IV. RESULTS AND DISCUSSION

The proposed Digital Space Vector PWM (DSV-PWM) module is designed and implemented on Artix-7 FPGA for 3Φ-VSI applications. The DSV-PWM is designed using Xilinx ISE 14.7 Environment with Verilog HDL and simulated on Modelsim 6.5f Simulator. The DSV-PWM is implemented on Artix-7 FPGA with the device of XC7A100T-3 CSG 324. The DSV-PWM Module provides low-cost FPGA implementation with high performance. The simulation results of the DSV-PWM Module are represented in Fig. 8.

Once clock (clk) is activated with active-low reset (rst) signal, The DSV-PWM operation starts. The 3-bit select line (sel) is used in the Sector generation module to perform the signed shifting operation. The 3-phase va, vb, and vc are 8-bit voltage inputs and generate the DSV-PWM outputs like xd and xq by Xqd Module 8-bit outputs, 3-bit selection generation output, t0, t1, and t2 are 8-bit switching time outputs and final pa, pb, pc are PWM outputs.

The PWM outputs are generated based on 3-Phase voltage inputs along with sector generation and switching time module. The Resource utilization of DSV-PWM is generated after synthesis operation in Xilinx Tool. The DSV-PWM resource utilization in terms of Chip area, Timing analysis, and power Utilization are tabulated in Table IV.

The DSV-PWM utilized slice register of 27, slice LUT's of 337, and LUT-FF pairs of 27 on Artix-7 FPGA. The DSV-PWM module works at 597.83MHz with a minimum period of 1.67ns and a combinational delay of 2.17ns. The power utilization is analyzed for the DSV-PWM module using the Xilinx Xpower analyzer, and it consumes the total power of 110mW, which includes the static power of 82mW and dynamic power of 28mW. The overall power utilization of DSA-PWM is 100mW, which is quite less and suitable for real-time power electronics applications.

The DSV-PWM module contains four main sub-modules, namely, Xdq Module, Sector generation module (SGM), Square root Module (SRM), and CSA module. The slice – LUT's and the Combination delay of DSV-PWM sub-modules are tabulated in Table V. The X_{dq}, SGM, SRM, CSA utilize 24, 42, 8, and 12 slice LUTs respectively. Similarly, the Xdq, SRM and CSA have a combinational delay of 2.1ns, 1.74ns, and 2.52ns, respectively. The remaining Slice –LUT's of DSV-PWM Module are utilized by the Switching time module and PWM generation Module.

The proposed DSV-PWM is compared with similar existing SV-PWM technique with better improvements in design and hardware constraints. The DSV-PWM module is compared with existing SV-PWM [23] and is tabulated in Table VI for resource constraints.

The DSV-PWM improves around 69%, 14%, and 57% of less overhead in Slice registers, Slice LUTs, and Maximum frequency (MHz), respectively than the existing SV-PWM [23] technique. Similarly, the DSV-PWM dynamic power utilization by using different clock frequency is compared with existing SV-PWM [23] with better improvements is tabulated in Table VII, and graphical representation is showed in Fig. 9.

The DSV-PWM consumes the dynamic power of 7, 14, 21, and 28mW, which is quite less compared to the existing SV-PWM [23] technique with 23, 28, 33, and 37 mW against clock frequency of 25, 50, 75 and 100 MHz respectively.

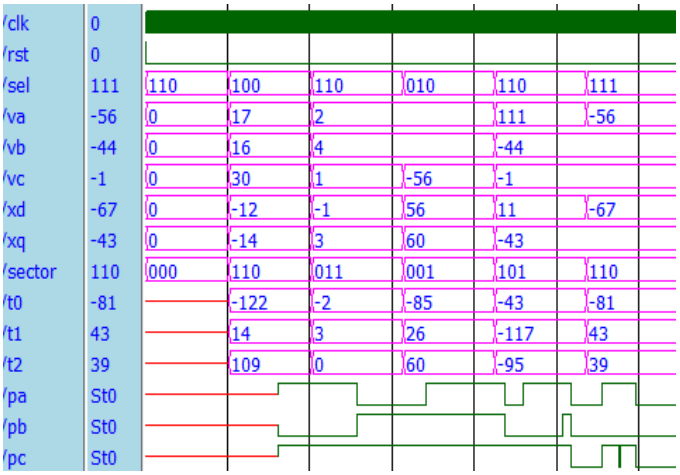

Fig. 8. Simulation Results of DSV-PWM Module.

TABLE IV. HARDWARE RESOURCE UTILIZATION OF DSV-PWM MODULE ON ARTIX-7 FPGA

Resources	**DSV-PWM**
Chip Area	
Slice Registers	27
Slice LUTs	337
LUT-FF pairs	27
Time	
Minimum period (ns)	1.673
Max. Frequency (MHz)	597.836
Combinational Delay (ns)	2.17
Power	
Dynamic Power (W)	0.028
Total Power (W)	0.11

TABLE V. SLICES LUT'S AND COMBINATIONAL DELAY (NS) OF DSV-PWM- SUB MODULES

Sub Modules	**Slice LUTs**	**Combinational Delay (ns)**
X_{dq} Module	24	2.106
Sector Generation Module	42	NA
Square Root Module	8	1.747
CSA Module	12	2.523

TABLE VI. RESOURCE COMPARISON OF DSV-PWM MODULE WITH [23]

Resources	**Ref [23]**	**Proposed**
FPGA Device	Cyclone II	Artix-7
Slice Registers	88	27
Slice LUT's	392	337
Max. Frequency (MHz)	253.85	597.836

TABLE VII. DYNAMIC POWER (MW) COMPARISON OF DSV-PWM MODULE WITH [23]

Clock Frequency (MHz)	**Dynamic Power (mW)**	
	Ref [23]	*Proposed*
25	23	7
50	28	14
75	33	21
100	37	28

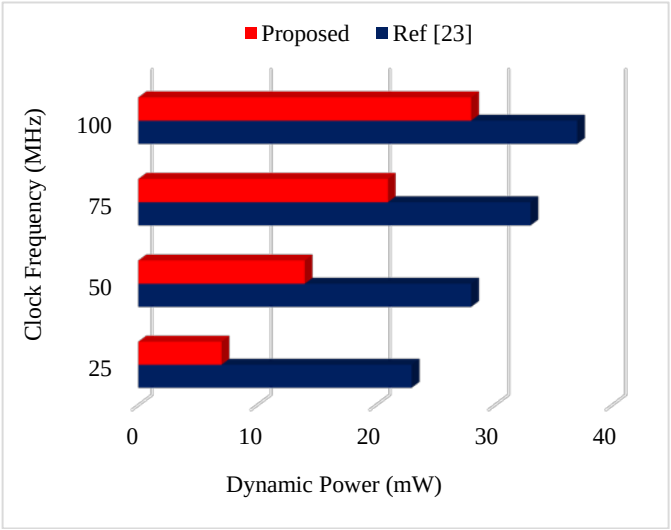

Fig. 9. Graphical Representation of DSV-PWM Dynamic Power (mW) by Concerning [23].

V. CONCLUSION AND FUTURE WORK

The DSV-PWM module is designed and implemented in Artix-7 FPGA. The DSV-PWM Module contains Xdq Module, Sector generation module (SGM), Switching time module, and PWM Generation Module. These modules are designed using simple logical operators and combinational circuits, which improve the hardware constraints like chip area, Power and frequency along with the performance. The DSV-PWM uses less chip area (< 1%), 110 mW total power and works at 597.836 MHz operating frequency on the FPGA device. The DSV-PWM method is also compared with the existing SV-PWM method with more considerable improvement in chip area, Frequency, and Dynamic power. In

the future, The DSV-PWM will be used in real-time power electronics applications and also to optimize the hardware constraints.

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