A Novel Low Power, Minimal Dead Zone Digital PFD for Biomedical Applications

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***Abstract*—Chronic diseases and rising aging populations are the major reasons towards the usage of low power, low noise, life time performance Biomedical Implantable Devices. Efficient architectural designs will be responsible for the requirements set out above. This paper focuses on the ADPLL DPFD architecture for implantable biomedical devices. For high performance DPFD, the dead zone, lock in time is a seldom limitation to ADPLLs. In the present paper, a new approach to design a dead zone free with fast and high locking time and low phase noise DPFD is considered to be a challenge. This can be accomplished by carefully controlling the reference and feedback clock frequencies of the phase detector with the proposed NIKSTRO/SURAV latch based sense amplifier. The proposed architecture was developed and simulated using 45nm technology and it is observed that it provides a 20ns dead zone with 4.8mW of power consumption at the rate of 1.8GHz, while the lock in time for the proposed method is 340ns with moderate phase noise. It is also noted that the designed one showed better results when compared to the existing ones.**

Keywords*—Biomedical Implantable Device (BIMD); Digital Phase Frequency Detector (DPFD); Digital Controlled Oscillator (DCO); Sense Amplifier Based Flip-flop (SAFF); NIKSTRO or SURAV

I. Introduction

Archeological research reveals that the Greek civilization used instruments to study the human body in order to understand human anatomy and to treat healthy and pathological conditions. This idea has placed roots for the growth of a biomedical tree. In addition to this, the technical advancements throughout medical sciences have always played an important role by making remarkable advances in health care resulting in emerging a field called biomedical engineering. The new science and technology of biomedical engineering have contributed to the manufacture of cutting-edge biomedical implantable over the last five decades, helping to improve clinician's know-how to improve the human anatomy [1]. A more precise diagnosis, which can be achieved by highly technical biomedical devices / BIMD's, is necessary for medical professionals to prescribe an effective cure. These BIMDs range from sensors, GES and cardiac pacemakers, ICD, to DBS, nerve (PNS, SCS), and bone stimulators.

While a variety of biomedical implants exist for many applications, each IMD consists mainly of an electronic system and battery [2]. Because of the IMD area and size limits, a Chip Specific System (AS-SoC) system is currently covering main portions of the IMDs. The main functionality of these devices is to monitor and analyze body physiological signals, to deliver the drugs needed precisely if necessary, to resurrect the malfunctioning organ or body part, for transmission of the diagnostic data, to receive the external commands, to stimulate the body's organ while it is not functioning properly, thus transceiver is the most important component in BIMDs. Conventional devices have been used for short-range magnetic IMDs that are easily affected by EM way interference resulting in transmission imprecision [3]. In order to provide the safety measures, whole ball of wax the medical applications should be carried out at Medical Implant Communication Services (MICS) ranging from 401 MHz to 406 MHz (intra range is 402 MHz to 405 MHz). The key building block in BIMDs is PLLs, but the conventional analog PLL's need a wider silicon area to accommodate LC oscillators, charge pump and RC LPFs and therefore not easily portable to other technology nodes. To overcome the analog PLL drawbacks, All Digital PLLs (ADPLLs) have been proposed. For detailed information on, How ADPLLs subtle the PLLs & Digital PLLs (DPLLs)? block diagram of PLL, categories of DPLLs, reader has suggested to read [3-8].

II. All Digital Phase Locked Loop

The advancements in CMOS technology scaled down the supply voltages $\leq$ 1 V, making the traditional analog PLL design for designers in current deep-submicron CMOS processes very challenging. Nevertheless, short channel CMOS process has preferred digital circuits and is therefore highly focused on digital circuits today. All these distinct factors lead to undergo a change in velocity of the growth of ADPLLs in which all the sub-blocks of the conventional analog PLL were replaced by their comparable/equivalent digital blocks. The general ADPLL block diagram is shown in Fig. 1 consisting of Digital Phase Frequency Detector (DPFD), loop filter and Digital Controlled Oscillator (DCO).

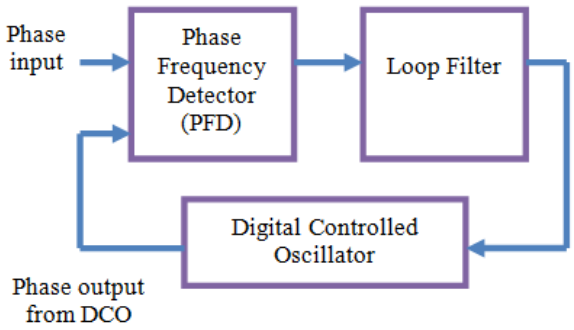


Fig. 1. General Block Diagram of ADPLL.

As all ADPLL blocks are digital, a converter is needed for designers' final analysis. An alternative approach in the current paper is also listed like Time to Digital Conversion (TDC) based ADPLL, which translates time intervals to a digital value to reduce the number of converters in ADPLL rather than using DPFD [4]. ADPLL's block diagram can now be modified slightly by using TDC in Fig. 2. Therefore the alternative ADPLL contains mainly the Time to Digital Converter (TDC), phase error detector (PED), the digital loop filter (DLF) and the computer controlled oscillator (DCO) with additional circuitry based on the requested application.

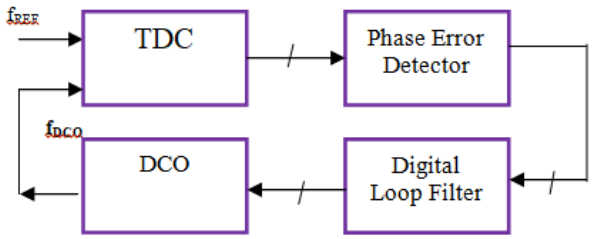


Fig. 2. Block Diagram of ADPLL with TDC.

III. Literature Survey

An alternative solution is important to overcome the design challenges of digitally driven deep-submicrometer CMOS processes. One of the solutions to dealing with the above listed problem is the time mode signal processing (TMSP). It operates and processes analog signal information through digital blocks, in which voltage (V) and current (I) variables are replaced with the appropriate time differences between two rising edges as the time variables, the large and power-hungry analog blocks can be substituted with logical circuits. In addition, digital elements as an analog circuit replacement, allows the use of digital synthesis and testing techniques. This represents significant step forward to bridge the gap between analog and digital design, which for the analog design community is extremely important. There are two types of converters known as DTC and TDC to offer the requirements mentioned. A TDC converts the time interval between the two clock edges to a digital number. Whereas the DTC is quite opposite to the TDC. For the detailed principle of operation of TDC [5, 6]. In ADPLL, the frequency comparator known as the Phase Frequency Detector (PFD) is replaced by the TDC. Various types of TDCs are available; some of them are taken into account and shown as appropriate in this paper.

Buffer delay line TDC (BDLTDC) [6], which can transmit signal via chain of buffers and flip-flops to output buffers. Once the reset signal is activated the delay line is sampled by flip-flops. Complete implementation is in digital, so it is very simple and easy to operate, but having lower resolution since it has the delay of one buffer cell.

Inverter delay line TDC (IDLTDC) [6], the signal transmission can take place through a chain of inverters and flip flops which can increase the resolution twice in comparison with BDLTDC but is therefore limited in applications by the advancements in CMOS technology.

Time to Amplitude Converter TDC (TACTDC) [7], is the combination of TAC and ADC (Analog to Digital Converter), the entire operation depends on the charging mechanism of a capacitor on the output section of the TAC. The capacitor value is then converted into a digital value with the help of ADC. Very simple to implement is the major advantage for ASICs, but they have a large dead time and the limited resolution for ADC operation, a high power dissipation for 50 ps resolution [7]. Because of its complete analogy in its structure designing, it has no CMOS implementation.

Vernier Delay Line TDC (VDLTDC) [6, 7] can measure the delay line with sub gate resolution mechanism. This architecture delays both START and STOP signals with uneven time periods (delay of STOP signal is slightly greater than the START signal) which is the START signal that leads the STOP signal. The operation explains that the resolution depends on the two delay lines rather than the delay element compared to BDLTDC, IDLTDC and TACTDC. VDLTDC provides not only high resolution, but also high power consumption and silicon area since it is composed of 2 buffers and one flip flop in its designing.

According to TDC's report, it drastically reduced the number of ADPLL converters required, but the remaining technical limitations were severely affected [3-7]. These results make TDC based ADPLLs were not suitable for bio-medical applications, but ADPLLs are the major functional unit in BIMDs, and there is a need for significant improvement in this area. Another major requirement for these types of devices is not only provision of ultra-low power consumption to safeguard a longer battery life, but also the provision of better circuit topologies for smaller silicon-area. One of the best ways to achieve ultra-low power consumption is to assertively scale down the supply V_{DD}, because the transition power dissipation of digital architectures has squared dependence on V_{DD} with constant capacitance and frequency for the same technology (CV^2F). Conversely, this destructive reduction in V_{DD} leads in low driving capability and reduced circuit speed due to threshold voltages of MOS devices. To overcome this, the working operation of MOS devices should be very close to the week/middle inversion region [9, 10]. Nonetheless, the mixed signal processing circuits functioning in these regions still shows the signs of low driving and switching speeds. In order to acquire low power consumption, less silicon-area and portability which are extremely required for the BIMDs, the use of TDC based ADPLLs should be bypassed.

The PFD [8] consists of two D flip - flops, a NAND gate and a reset path with a fixed delay element. The design process requires a large area of silicon and affects the dead zone due to the fixed delay cells.

A further signal called "dir" is given in PFD [10], which shows the leading and lagging information for clock phases. Additional circuits compared to the design shown in [8] are needed for the construction of this kind of PFD. D flip flops with Strollo's latches, which produce glitches at the PFD output. The overall architecture is complex and high power consumption. PFD-based ADPLL is therefore the best solution for biomedical applications, since it provides good qualitative and quantitative measurements for the required operation.

A new ADPLL consisting mainly of the digital phase Frequency detector (DPFD) rather than the TDC is introduced and discussed in this paper. A new approach to building the DPFD with SAFFs was considered. This paper is organized as, Section 1 deals with the introduction and the genesis of BIMDs, Section 2 presents the glance about the devices used in ADPLL with their pros and cons, following the literature survey of TDCs & PFDs in Section 3. Section 4 deals with SAFF and its operation with different latches, Section 5 provides information on the evolution and operation of proposed latch, Section 6 provides a description of the design of DPFD with the proposed SAFF, finally a comparative conclusion as set out in Section 7.

IV. Sense Amplifier based Flip Flop (SAFF)

Daily use of electronic devices in various applications in different fields has led researchers to work on new ideas. SAFF is one of the proofs of the requirements set out above, since it has been used in digital systems where high performance, high reliability, high speed and low energy consumption are the primary criteria. The limitations of timing elements, storage elements such as (latches and flip-flops) and clock loading make SAFF the key choice for most applications in the digital era. The above parameters are partly or entirely depending on the clocking mechanism. Due to the fact that clock distribution network and the impact of the clock skew, setup time, hold time and their relationship in the design consumes 20 to 45% of the total power consumption of the digital system [11], imposed on new latches and flip flop designs.

A. SAFF Mechanism

The standard flip-flops consist of pulse generators followed by a latch as shown in Fig. 3: the schematic representation appears to be the same as the master-slave flip-flop, but varies in its operation.

From Fig. 3, the pulse generator sets the operation of the slave latch by generating pulses of sufficient duration on the basis of input data and clock signal considerations. Depending on the specific time of increase of the clock signal and the time of dropping, the pulse generator stage is more sensitive to the edges than to the depths. This may give rise to an ambiguous situation for the operation of a flip flop under certain conditions, mainly in terms of reliability and robustness of operation. Thus, some design methodologies such as IBM's LSSD [11] struggled to allow use of flip flops.

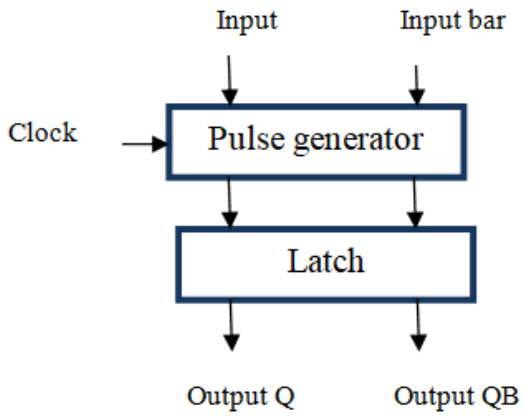


Fig. 3. Traditional Flip Flop Block Diagram [11].

SAFF also has master and slave blocks identical to flip flop, except the master block is a sense amplifier, and the slave block is a key, as seen in Fig. 4: Sense amplifier block is the name given because it is sensed with a clock signal and additional differential inputs and produces complemented inputs to the slave latch. Slave latch is designed as an SR (Set-Reset) latch that has been ignited by either SB or RB (but not both) created by the master block [11-16].

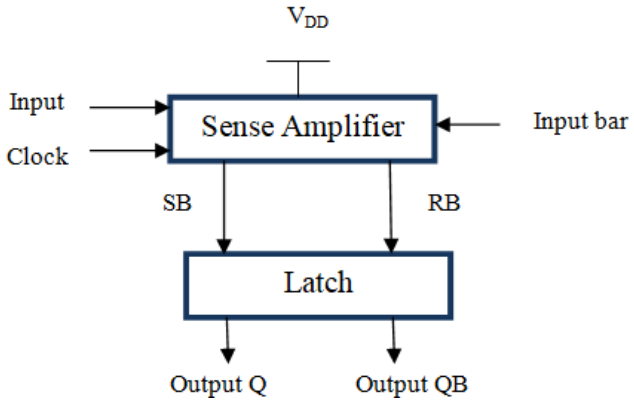


Fig. 4. General Structure of SAFF.

The entire design of SAFF portrays the flip flop process as the Sense amplifier block produces uniform transitions from logic zero to logic one on any output based on the leading edge of the clock distribution. During the clock operation, the output is not affected by any successive changes to the input data. The output state generated can now be processed and the slave latch can be held until the next leading edge of the clock signal arrives. Once the clock is inactive, both outputs of the master block assume high logic [11-16].

B. Operation of Sense Amplifier

The operation of the Sense Amplifier stage is mainly controlled by the clock signal as follows:

When the clock is in an active low state: then the PMOS transistors PM1 and PM4 are ON, the output nodes SB and RB are precharged to logic high (H). Both states make NMOS transistors NM1 and NM2 ON and charge their sources to VDD-V_{thNMOS}, since there is no clear path to the ground due to the clocked NMOS transistor NM5 being OFF. The common NA node (NM3, NM4 and NM5) will also precharge either

NM3 or NM4 to VDD-V_{thNMOS}. Thus, all the MOS capacitances in the differential tree were precharged before the clock signal enters the logical high level.

When the clock is in the active high state (H): the NMOS transistor NM5 is completely ON-conditioned, creating a direct path to SB and RB towards the ground, conditioned on the status of the NM3 or NM4 transistors. The detailed SB is discharged by either NM1, NM3 & NM5 when D is logic H by turning NM2 OFF and PM3 ON or NM1, NM6, NM4 & NM5 when DB is logic L which is the longest delay path for discharging (not preferable for high-speed applications). The smallest path for RB is through NM2, NM4 and NM5 when DB is logic H by turning NM1 OFF and PM1 ON. Further alterations of input data should not affect the status of SB and RB after these initial changes [11-16]. The complete operation of sense amplifier can be described in Table I.

Another important observation in Fig. 5 is that the inputs are decoupled from the outputs of the sense amplifier stage forming the basis for the flip flop operation of the circuit [12]. All transistors were designed using 45 nm technology, considering that all PMOS (PM1 to PM4) had a W / L ratio of 4 units and NMOS (NM1 to NM6) had 2 units. The resulting increase time and fall time in the simulated waveforms is approximately 40ns and therefore the total propagation delay is almost 20ns. In order to obtain a DB signal, the data D signal is inverted with a delay element having the same W / L ratio for PMOS and NMOS.

At the high clock pulse, the output of the sense amplifier forces to low, and this will be floating low if the data changes during the high clock pulses. Although the data is modified, the NM6 transistor provides a path to the ground that prevents the possible charging of the low output of the sense amplifier stage due to leakage currents. These leakage currents cannot be ignored in the low power design. The other important observation of the NM6 transistor is that it irregularly charges and discharges the entire differential section of the master stage during each clock cycle without any reference to the data input at the leading edge of the clock as shown in Fig. 6(a). This simultaneous charging and discharging slow-down operation of the sense amplifier must be minimized in the design for the prevention of NM6, as shown in Fig. 6(b).

C. Operation of Slave Latch

The symmetrical NAND (traditional structure) [11] or NOR logic can be used to create a slave latch. Slave latch treats SB as a set and RB as a reset input in traditional SAFF. Q, QB depends on SB, RB as SB sets Q to H, which forces QB to L, and RB sets QB to H, which forces Q to L. Therefore, one of the outputs of the slave latch will always lead the other if the latch is implemented using CMOS logic NAND gates contributes to a SAFF performance limitation.

A new slave latch that should have symmetry functionality is required to solve the question of the conventional implementation. In the technical market there are various types of latches to select the right one. The best latches for power consumption circuits include the latches such as Nikolic's [11-13], Kim's [17], Strollo's [18]. Comparative parameters such as rise delay, fall delay, power consumption and power delay product (PDP) descriptions of these latches are shown in Table II. From the table, the latch of Strollo's is a bit faster than the rest of the latch in case of a fall delay, which makes PDP too low compared to others. But in case of rise delay, Nikolic's latch comes first after Kim's and Strollo's latches. In terms of power consumption, Strollo's consumption is about 7.5% lower than Nikolic's, as shown in Table II.

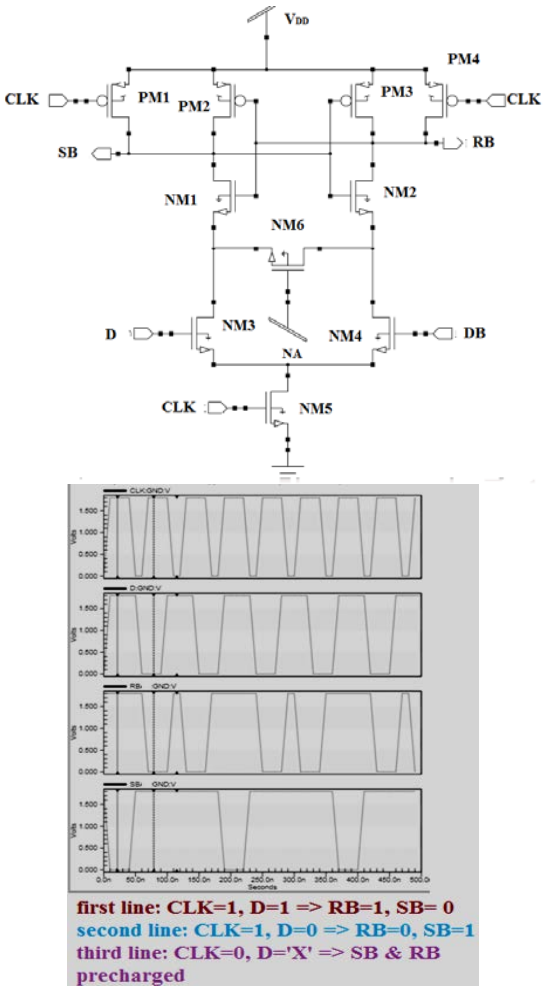
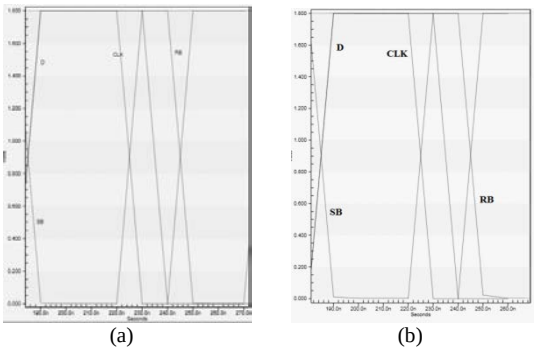


Fig. 5. Sense Amplifier in SAFF and its Simulation Waveform (Simulated using 45nm Technology).



(a) (b)

Fig. 6. Simulation Waveform of a Sense Amplifier (Over a Period of Sample Provides CLK-Q Delay and CLK-D Delay for both Transitions) (a) Including NM6, (b) Excluding NM6.

TABLE I. TRUTH TABLE OF SENSE AMPLIFIER

CLK	D	DB	SB	RB
0	X	X	PRECHARGED	PRECHARGED
1	0	1	1	0
1	1	0	0	1

TABLE II. PERFORMANCE COMPARISON OF SAFFS WITH DIFFERENT LATCHES

Parameter	Nikolic's [11]	Kim's [17]	Strollo's [18]
Number of transistors	28	26	24
Rise delay(ps)	265	221	285
Fall delay(ps)	236	231	161
Power consumption (µW)	480	425	444
Power Delay Product (PDP) (fJ)	127	98	99
Glitch free output[18]	Yes	No	Yes
Ratio less	Yes	No	Yes
Q and QB delay independence	Yes	Yes	Yes
Dual outputs	Yes	Yes	Yes

V. PROPOSED LATCH

A. Design of Proposed Latch

This paper, based on the new concept-a hybrid solution-will lead to the best architecture with the nominal parameter values through Nikolic's latch design principle and Strollo 's logic functionalities. The hybrid-symmetric structure was constructed based on Table III of the SAFF truth table. It has been constructed in 4 sub-parts with 2 pull-up (PUN1 and PUN2) and 2 pull-down (PDN1 and PDN2) parts. These sections are cross-coupled as PDN1 × PUN2 and PDN2 × PUN1 and this orientation results in a small design transistor requirement compared to conventional latch.

The output Q(next state output) of the proposed latch can be obtained from the CMOS pull down network (PDN1) given in (1) and the CMOS pull up network (PUN1) given in (2).

$$((CLK.DB+QB)SB) \quad (1)$$

$$((CLKB+DB)\,QB+R) \quad (2)$$

Similarly, for QB(next state output) obtained from CMOS, pull up the network (PUN2) given in (3) and pull down the network (PDN2) given in (4).

$$((D+CLKB)Q+S) \quad (3)$$

$$((CLK.D+Q)RB) \quad (4)$$

It is quite obvious from the Boolean equations that these were derived from the NIKOlic design theory and from STROllo Boolean equations so that the name of the proposed latch was described in the form of the NIKSTRO latch or the SURAV latch (because it was designed/proposed by SUdhakiran G and ernest RAVindran R S).

B. Operation of NIKSTRO/SURAV Latch

As the proposed architecture working with differential signals then from Table III, when output Q rises to logic high, then the signal R remains at logic low and RB is in logic high even though they have an inverter delay. In the pull down section of proposed latch that is equivalent to Strollo's latch, the transistors NM1, NM2, NM3 provides the discharging path to the output Q as soon as the clock transitions are from low to high and the QB discharges through NM6, NM7, NM8 so that one delay gate is needed for the proposed architecture [18].

TABLE III. TRUTH TABLE OF SAFF

CLK	D	DB	SB (from SA)	RB (from SA)	S	R	Q	QB
0	X	X	1	1	0	0	NC	NC
1	0	1	1	0	0	1	0	1
1	1	0	0	1	1	0	1	0

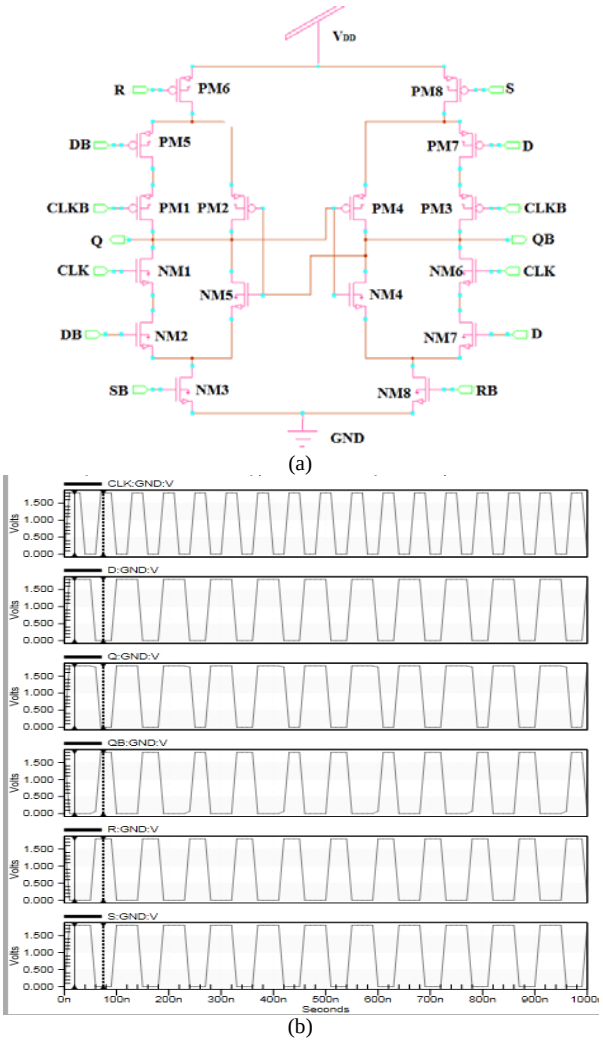


Fig. 7. (a) Proposed Latch (Nikstro Latch) Structure (b) Waveforms of Nikstro Latch.

The transistors PM2, NM5 and PM4, NM6 are constitute a cross coupled inverter structure which provides the present states, outputs to the next state inputs for the operation of the latch. In the pull up section of SURAV Latch, the additional transistor PM5 is to avoid the glitches at the output. If the clock is logic low, then the MOS transistors PM1, PM3, PM6, PM8, NM3, NM8 are ON and NM1, NM6 are OFF, based on these values the cross coupled inverter sections are also in ON such that the architecture retains the logic values. When CLK is high the output Q of SURAV latch charges through PM6, PM5 and PM1which are controlled by R, DB and CLKB respectively. Similarly QB charges through PM8, PM7 and PM3, which are controlled by S, D and CLKB, respectively. Fig. 7(a) and (b) represents the proposed NIKSTRO structure and its simulated waveforms. During the simulation complement signals can be generated using an inverter. Table IV specifies the transistor aspect ratio in the Surav latch.

TABLE IV. W/L RATIOS OF MOS TRANSISTOR IN THE PROPOSED LATCH

MOS transistors	W/L ratio
PM1 – PM8	4
NM1 – NM8	2
Inverters (additional) PMOS NMOS	 4 2

C. Algorithm for Designing and Operating NIKSTRO/SURAV Latch

Step 1: Inputs for the NIKSTRO latch have been obatined from the Sense Amplifier section.

Step 2: According to the truth table obtained from Step1 the slave latch pull down network implemented by Strollo's Logic.

Step 3: According to the truth table obtained from Step1 the pull up network of slave latch implemented according to the Nikolic's latch in concerning with Step 2.

Step4:A hybrid slave latch is developed after Step 3 and is named as NIKSTRO / SURAV latch.

Step 5: Operation of slave latch is:

if (CLK=1) **then**

if (D=1) **then**

Q=1 and QB=0 (intermediate signals S=1 and R=0)

else

Q=0 and QB=1(intermediate signals S=0 and R=1)

else

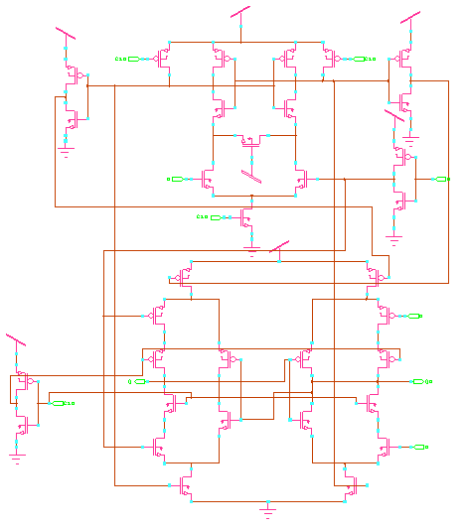
Q= previous output and QB=previous output

Step 6: The operation of the proposed latch is exactly the same as the normal latch

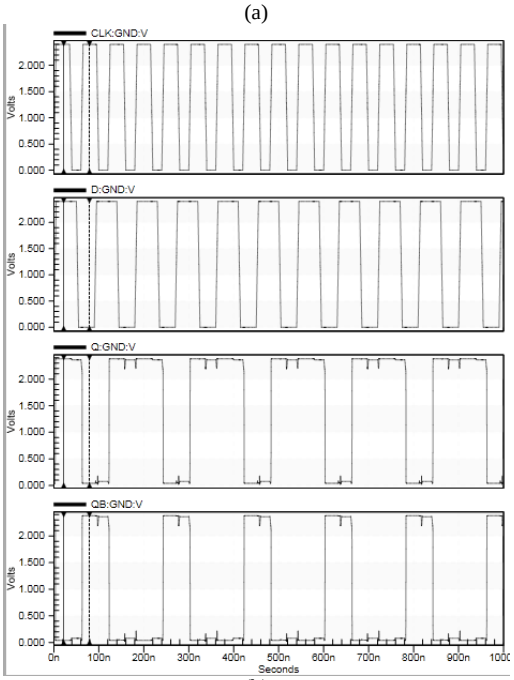
D. Sense Amplifier based Flip Flop with NIKSTRO Latch

This is also called a flip-flop due to its function because it uses latch in the construction of SAFF. From Table III, it is very clear that the latch can capture and sustain the transition to the next rising edge of the CLK signal. The two outputs of the sense amplifier stage are considered to be normal when the CLK reaches a true low level. The whole idea therefore turns out to be flip-flop. The designed and simulated SAFF is shown in Fig. 8(a) and (b), respectively. Fig. 8(a) is complex to understand, the condensed and rearranged diagram shown in (c) is very similar to Fig. 4.

The NIKSTRO latch SAFF will only be ready for real-time applications when it operates efficiently with synchronous and asynchronous signals. Nikstro SAFF with synchronous signals discussed in the Section V. Now this is the right time to disclose the operation of the proposed SAFF with asynchronous signals-preset and clear. The circuit diagram shown in Fig. 9(a) illustrates how the asynchronous preset (PRST) and clear (CLR) signals connected to the proposed SAFF in Fig. 8(a). Fig. 9(b) represents the simulated waveforms of the proposed SAFF with asynchronous signals (considered PRST= 0) affecting the Q and QB output glitches and having a high processing time of 102ns.



(a)



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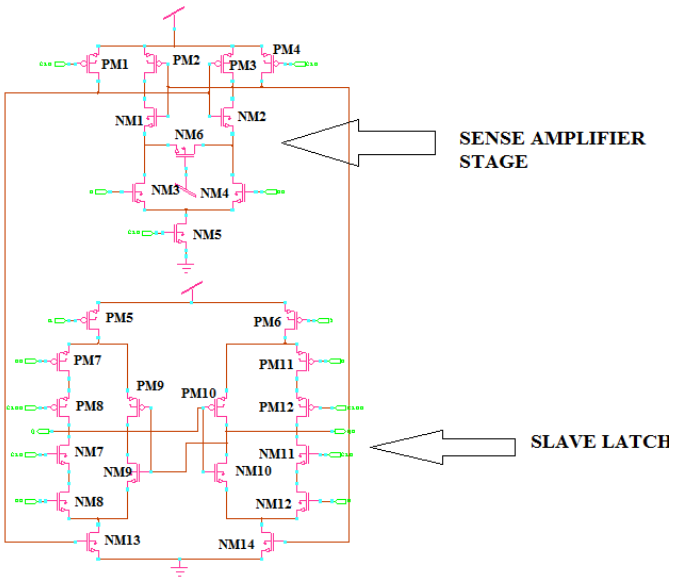
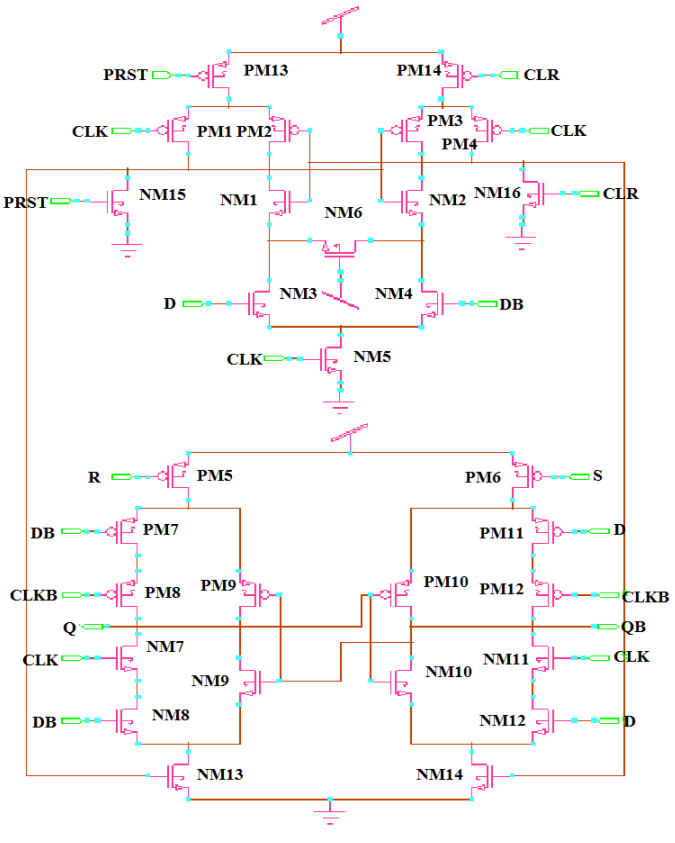
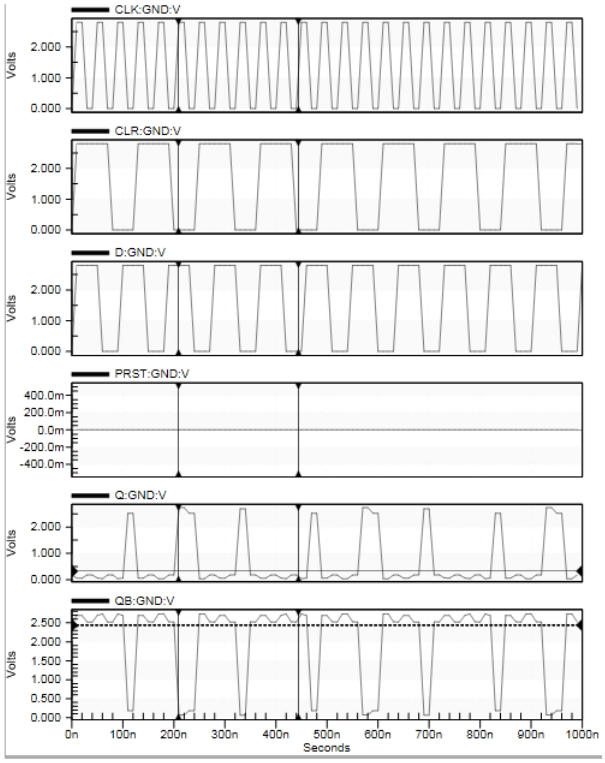


(c)

Fig. 8. Proposed SAFF with NIKSTRO Latch (a) Design (b) Simulated Waveforms (c) Simplified SAFF with NIKSTRO Latch.



(a)



(b)

Fig. 9. Proposed SAFF with Asynchronous Signals Preset and Clear (a) Design (b) Waveforms (with Preset Signal Value Zero).

VI. Digital Phase Frequency Detector (DPFD)

ADPLL's overall performance is contingent on each block's output contribution. The main blocks in ADPLL are DPFD, Digital Loop Filter (DLP), Digital Control Oscillator (DCO) as shown in Fig. 10.

Parameters such as phase noise minimization, low noise and fast ADPLL lock can mainly be obtained from DPFD. This can only be accomplished by properly organizing and observing the input reference signals (pf_{REF}) and the signal produced by the DCO (pf_{DCO}). In reference to the frequency and phase of the input reference signal and the DCO feedback signal DPFD produces the output signal (UP and DOWN). The difference between UP and DOWN signals increases the phase noise of the DPFD and modulates the output that alters the entire activity of the ADPLL [20]. The conventional PFD must provide fast locking, high operating speed and low dead zone [21, 22]. The only way to achieve the above properties for ADPLL is to concentrate and properly manage the dead zone condition. The main goal of this paper is to reduce the dead zone situation to the minimum possibility. It can be achieved by simultaneously increasing the output signals of the DPFD when it is locked. The ideal PDF diagram is shown in Fig. 11.

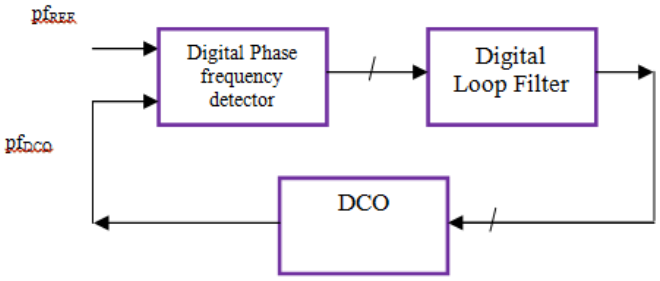


Fig. 10. General Block Diagram of ADPLL [19].

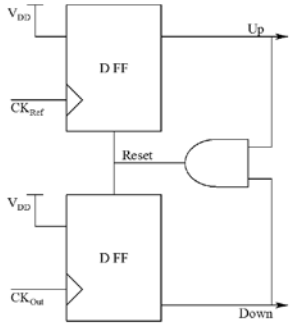


Fig. 11. Conventional Digital Phase Frequency Detector [20-22].

Old PFD methods used to reduce the dead zone, by keeping the fixed delay element [21-23] or variable delay element [20] in the reset path. But these procedures trigger disruptions in the control voltage of the oscillator leading to the reference spurs at the ADPLL output [20-24]. This paper focuses on a novel approach to provide the dead zone free and low phase noise architecture for DPFD. Initially, the produced UP and DOWN DPFD signals are low, once the clock of any flip flop rises, the outputs are enabled accordingly. This can be continued until the output of the other flip flop is going to high. When the two output signals are high, the entire circuit is reset. The DPFD performance of charging and discharging depends on the clock frequency of flip flops. Ideally, there should be a linear relationship, but it basically varies. The phase difference changes when the frequency changes since they are related as shown in (5) [20].

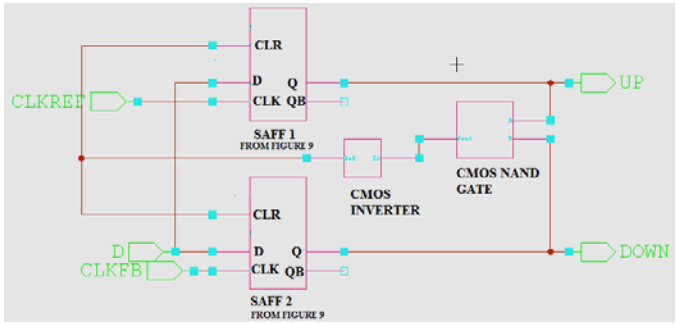
$$\Delta\varphi = 2\pi\left[\frac{t_{pf_{ref}} - t_{pf_{DCO}}}{\max\left(t_{pf_{ref}}, t_{pf_{DCO}}\right)}\right] \quad (5)$$

Where $t_{pf_{ref}}$ and $t_{pf_{DCO}}$ are the time periods of the input reference signal and DCO feedback signal.

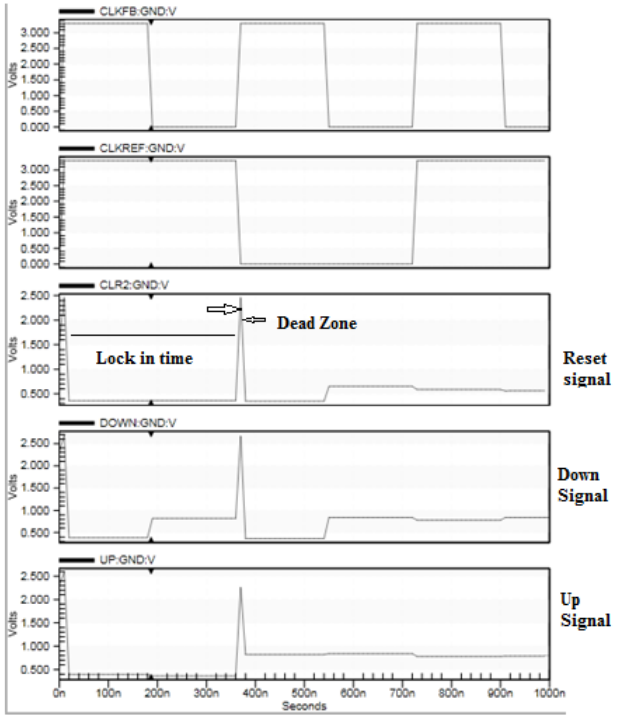
These incoming signals determine the set or reset condition of DPFD. If ADPLL is in locked state, then the phase difference between these two signals is much less. During this condition if any of the flip flops received the raising edge, then it will set and produce the high output. Meanwhile, if another flip flop detects the rising edge then it will also set and produce the high output. Thus the two outputs of DPFD are high which causes a reset signal for the flip flops and makes DPFD disable for the phase difference detection. This phenomenon is called as a dead zone in which the DPFD is unable to detect the phase differences which are smaller than the dead zone leads increase in overall phase noise of ADPLL. The conventional PLLs have a divider in its feedback path which relates the phase noise spectral density which has a strong relation between phase noise and the delay width (T_D) of the delay element. Therefore, phase noise cannot be decreased below a certain amount without reducing the dead zone [20]. The novel approach which uses a low power, high robust architecture is introduced here to reduce the dead zone of ADPLL. The proposed DPFD is implemented using the Sense Amplifier based flip flops (SAFF) shown in Fig. 9. The implementation block diagram and its simulated waveforms are shown in Fig. 12(a) and (b) with preset signal is set to zero since preset requirement is not required in DPFD operation.

For the designing of PFD, the W/L ratios can be taken from Table V for SAFFs and for CMOS inverter and NAND gate the W/L ratio for PMOS is taken as 4 and for NMOS 2 it is based on the drain to source current I_{DS} is given in eq. 6.

$$I_{DS} = \frac{k}{2}\frac{W}{L}\left(V_{GS} - |V_{T_n}|\right)^2(1 + \lambda V_{DS}) \quad (6)$$



(a)



(b)

Fig. 12. Proposed DPFD with Preset Signal Setting to Zero (a) Block Diagram (b) Waveforms.

Where k is a process gain factor = $\frac{\mu\epsilon}{t_{ox}}$ μ,Ɛ and t_{ox} values depends on technology used, these values are different for PMOS and NMOS transistors.

$$\mu = \frac{average\ carrirer\ drift\ velocity}{electric\ filed}$$

λ – Is the empirical channel length modulation co-efficient.

The propagation delay in the mentioned architectures is calculated as.

$$\sum_{i=1}^{n} t_{pi} \quad (7)$$

n- Number of delay elements in the stages

t_{pi} - total propagation delay

The low to high transition (t_{pLH}) at the output can be derived as (similar approach is followed for high to low transition also (t_{pHL})). Therefore:

$$t_{pHL} = \frac{C_L\frac{V_{OH}}{2}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{n(p)}\left(V_{OH}-V_{T_{n(p)}}\right)^2} = t_{pLH} \quad (8)$$

where $C_L = C_G + C_P$

$V_{OH} = V_{DD}$

Equation 8 can be modified from equation 6 as follows

$$t_{pHL} \approx \frac{C_L}{k_n V_{DD}(1+\lambda V_{DD})} \quad (9)$$

$$t_{pLH} \approx \frac{C_L}{k_p V_{DD}(1+\lambda V_{DD})} \quad (10)$$

where k_n & k_p are the process gain parameters of NMOS & PMOS respectively

Therefore the propagation delay of an inverter is given as

$$t_p = \frac{1}{2}(tpHL + tpLH)$$

From equation 9 & 10 the propagation delay of an inverter is given as

$$t_p = \frac{C_L}{V_{DD}(1+\lambda V_{DD})}\left(\frac{1}{k_n}+\frac{1}{k_p}\right) \quad (11)$$

According to the number of delay stages used in the designing, the total propagation delay is calculated by using (7).

The clock to data and output delays provided by the circuit shown in Fig. 8(a) are: the clock to data (CLK – D) delay is recorded as 30ns for low to high transition and for high to low transition it took 15ns. Similarly for clock to Q (CLK – Q) the low to high and high to low transitions reported as 40ns and 22ns respectively. These delays are approximately equal to the delays caused by the voltage variable delay element PFD architecture [20] and the theoretical calculations done using (7) & (11).

VII. Performance Analysis

A. Proposed SAFF

The mixed transistor size was used in Fig. 9, details of which are shown in Table V, in order to achieve the right results. The figures in the table are the transistor's width / length ratio to the technology of 45 nm. The minimum transistor size is indicated by the * symbol.

TABLE V. W/L Ratios of MOS Transistor in the Proposed SAFF (L=45nm)

MOS transistors	W/L ratio
PM1,PM4	8
PM2,PM3	2.32*
PM5-8,PM11,PM12	11
PM9,PM10	2.32*
NM1, NM2	12
NM3,NM4	16
NM5	2.32*
NM6	24
NM7,NM8,NM11-14	11
NM9,NM10	2.32*

B. SAFF Performance Comparison

SAFF performance comparison with existing ones is given in Table VI and Fig. 13.

TABLE VI. Performance Comparison of SAFFS with Different Latches

Parameter	Nikolic's [11]	Kim's [17]	Strollo's [18]	NIKSTRO (proposed)
Technology	-	-	250nm	45nm
Number of transistors	28	26	24	26 (figure 8(c))
Rise delay(ps)	265	221	285	296
Fall delay(ps)	236	231	161	180
Power consumption (μW)	480	425	444	132
Power Delay Product (PDP) (fJ)	127	98	99	32
Glitch free output[18]	Yes	No	Yes	Approximately yes (figure 8(c))
Ratio less	Yes	No	Yes	Yes
Q and QB delay independence	Yes	Yes	Yes	Yes
Dual outputs	Yes	Yes	Yes	Yes

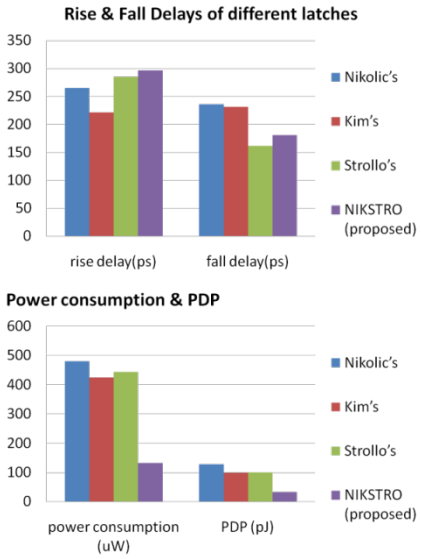


Fig. 13. Comparison of SAFF with different Latches.

C. Proposed DPFD

Fig. 12(b) shows the transient response of each signal in the DPFD proposed. This will make it very clear that the outputs of flip flops become active when the two clock signals are high. But this state cannot be sustained for a long time; within 20nsecs the clock signals receive other inputs. Therefore the dead zone for the proposed DPFD is 20ns. Another advantage of the proposed one is, it increases the lock-in time to 340ns such that it provides a bandwidth of 8.33 MHz's for locking operation. As the proposed architecture requires quite a bit large silicon area compared to the existing architectures, the stacking transistors have been forced to use the supply voltage between 2.915V to 3.3V. For the purpose of simulation, 3.3V was considered in this paper. As a result, the power consumption is marginally increased and results in a value of 4.8mw.

TABLE VII. DPFD COMPARISON WITH EXISTING ONES

Parameter	**[8]**	**[10]**	**[20]**	**[25]**	**[26]**	**[27]**	**[28]**	**Proposed**
Design	ADPLL	ADPLL	PFD	ADPLL	ADPLL	ADPLL	PFD	PFD
Technology (nm)	130	180	90	90	28	22	130	45
V_{DD}(V)	0.7	1.8	1.8	0.52/1	1	-	1.2	2.9 - 3.3
Lock in time (µs)	-	-	<1	0.8 (4 Cycles)	<1	12	-	0.34
Dead zone (ns)	-	-	36	-	-	-	52	20
Power consumption (mW)	0.84 @412 MHz	22.68 @1.26GHz	1 @500 MHz	0.92 @600 MHz	0.64	18.4	0.496 @128 MHz	4.8 @ 1.81 GHz

VIII. CONCLUSION

In the dead zone and the locking range with a little more power consumption, this approach obtained better performance. Dead zone and lock in time are recorded for this design. The lock-in-time for the new architecture is roughly 340ns, which is greater than the fixed delay architecture. Another advantage of the proposed one is that the dead zone area is about 20ns less than the architectures referred in Table VII. For the implementation the wide silicon area is needed as it requires more transistors in the design, which is a constraint on the proposal. A further limit for the proposed architecture is a high phase noise of order -8.9db/Hz. However, the cumulative analysis of all parameters reveals a marginally increased phase noise and power usage, with the design being best achieved with appropriate lock in time & dead-zone modulation. This takes a closer look on the proposed design to use in BIMDs.

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