

# Optimized Design of Decoder 2 to 4, 3 to 8 and n to $2^n$ using Reversible Gates

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**Abstract—**The design of low consumption CMOS circuits, nanotechnologies and quantum computing has become more attached to the reversible logic. A set of gates have been recently exploited in reversible computer science for the design of certain circuits. Among them, we find the decoders. In this paper we have exploited a recent study making the design of the decoder 2 to 4, 3 to 8, and n to  $2^n$ , our work aims to enhance the previous designs , by replacing some reversible gates by others while maintaining their functionality and improving their performance criteria namely the number of gates (CG), number of garbage outputs (NGO), number of constant inputs(NCI), Quantum cost (QC) and hardware complexity (HC), compared to our study of the base and other recent studies from which we have obtained remarkable results.

**Keywords—**Decoder 2to4; Decoder 3to8; Decoder n to $2^n$ ; Number of Gates (CG); Number of Garbage Output (NGO); Number of Constant Inputs (NCI); Quantum Cost (QC); Hardware Complexity (HC)

## I. INTRODUCTION

The energy consumed in the circuits presents a major problem revealed in many research studies that are in progress to design low power devices. The loss of energy in static and dynamic electricity consumption within a chip generates thermal dissipation. Moreover, referring to the Landauer principle [1], heat occurs due to the loss of information in any irreversible circuit. The higher the number of information losses, the greater the heat dissipation. In irreversible circuits from the output vector, one cannot uniquely deduce the associated input vector which results in a loss of information which in turn generates a heat dissipation of  $KT\ln 2Joules$  by bit loss, where K is the Boltzmann constant and T is the absolute temperature. The amount of heat loss seems small, but it will be large when a circuit contains a good amount of information loss. Bennett [2] in his research has proven that these heat generation problems can be resolved as long as the circuits could be designed with reversibility. There is no loss of information in the reversible circuits, and therefore a minimum amount of power dissipation. Today the need of reversible computing is important. Reversible computation is performed by reversible circuits. A quantum computer is quantum network composed of quantum logic gates; It has applications in many research areas such as Low Power Complementary Metal Oxide Semiconductor (CMOS) design, quantum computing, etc. All quantum gates are reversible gates and therefore quantum computing is one of the ways to design

low power circuits. There is a one-to-one mapping of input-output model in all quantum gates. Reversible circuits are those circuits whose outputs can be decided from the input template. quantum cost. The pattern of quantum circuit design is to minimize the amount of waste and reduce the quantum cost.

On the other hand [21-23] the decrease in energy dissipated at the end of unused bits because heat is directly related to less garbage outputs.

This paper will be organized as follows:

the 2<sup>nd</sup> section presents the reversible gates and their performance criteria, namely the quantum cost deduced from the associated quantum implementation, and the hardware complexity.

In the 3<sup>rd</sup> section, we exploit a design of each decoder 2 to 4, 3 to 8, and n to  $2^n$  from a recent article [13] we modify and show their associated performance criteria. To compare our new designs, we expose several designs from previous studies for comparison against our new designs of each decoder in terms of the 5 performance criteria CG, NGO; NCI, QC, and HC.

In the 4<sup>th</sup> section, we will present our design of the decoder 2 to 4, 3 to 8 and n to  $2^n$  and display 5 performance criteria while calculating the percentages of improvement obtained. finally, in the 5<sup>th</sup> section a conclusion and perspectives.

## II. THE REVERSIBLE GATES CONCERNED BY THE STUDY AND THEIR PERFORMANCE CRITERIA

In this section we will define the performance criteria concerned by this article which are in total 5.

### A. Performance Criteria:

1) *Number of Gates (CG)*: The number of gates required to make a circuit [3].

2) *Number of Garbage Outputs (NGO)*: The unused or unwanted logic outputs of the reversible gate maintain in the output lines to make the circuit reversible [3].

3) *Number of Constant Inputs (NCI)*: Number of inputs that must be remain constant at 0 or 1 to integrate the given logic function [3].

4) *Quantum Cost(QC)*: The QC is calculated by counting the number of a one input-output and two input-output reversible gates used in realizing a circuit [4,5]. The QC of a one input-output and two input-output reversible gates is realized to be 1.

5) *Hardware Complexity (HC)*: The number of fundamental operations (Ex-OR, AND, NO, etc.) required to make the circuit. actually, a constant complexity is supposed for each fundamental operation of the circuit, such as  $\alpha$  for Ex-OR,  $\beta$  for AND,  $\delta$  for NOT, etc. Eventually, the entire number of operations is calculated in terms of  $\alpha$ ,  $\beta$ , and  $\delta$  [6].

In this section we will present the reversible gates that are concerned by this paper by showing their performance criteria, namely the quantum cost that we deduce directly from the quantum implementation, and its hardware complexity.

#### B. Reversible Gates

1) *NOT Gate*: A reversible gate  $1 * 1$  having as inputs A and as outputs  $P = A'$  the quantum cost of the gate NOT gate is worth  $QC = 0$ , its Hardware complexity is worth  $HC = 1\alpha$  [3]

2) *Feyman Gate FG*: A reversible gate  $2 * 2$  having as inputs A and B and as outputs  $P = A$  and  $Q = A \oplus B$  the quantum cost of the gate FG is worth  $QC = 1$ , its Hardware complexity is worth  $HC = 1\alpha$  [3]

3) *Double Feyman Gate F2G*: A reversible gate  $3 * 3$  having as inputs A, B and C as outputs  $P = A$  and  $Q = A \oplus B$   $R = A \oplus C$  the quantum cost of the gate FG is worth  $QC = 2$ , its Hardware complexity is worth  $HC = 2\alpha$  [3]

4) *Fredkin Gate FRG* : A reversible gate  $3 * 3$  figure 1.31 having as inputs A, B and C and as outputs  $P = A$ ,  $Q = A'B \oplus AC$  and  $R = A'C \oplus AB$  the quantum cost of the FRG gate is equal to  $QC = 2$ , its Hardware complexity is equal to  $HC = 2\alpha + 4\beta + 1\delta$  [3]

5) *Peres Gate PG* : A reversible gate  $3 * 3$  figure 1.35 having as inputs A, B and C and as outputs  $P = A$ ,  $Q = A \oplus B$  and  $R = AB \oplus C$  the quantum cost of the gate PG is equal to  $QC = 4$ , its Hardware complexity is worth  $HC = 2\alpha + 1\beta$  [7]

6) *RI Gate* : A reversible gate  $3 * 3$  having for inputs A, B and C as outputs  $P = B$ ,  $Q = AB' + BC$   $C$  and  $R = AB \oplus C$  the quantum cost of the RI gate is equal to  $QC = 4$ , its Hardware complexity is worth  $HC = 1\alpha + 3\beta + 1\delta$  [8]

7) *HLGate* : A reversible gate  $4 * 4$  having as inputs A, B, C and D as outputs  $P = AB' \oplus B'C \oplus BD'$ ,  $Q = AB \oplus B'C \oplus BD$ ,  $R = A'B \oplus B'C \oplus BD$  and  $S = AB' \oplus BC \oplus B'D$  the quantum cost of the HL gate is equal to  $QC = 7$ , its Hardware complexity is worth  $HC = 7\alpha + 9\beta + 3\delta$  [9]

8) *NKHD Gate* : A reversible gate  $6 * 6$  having as inputs A, B, C, D, E and F as outputs  $P = A$ ,  $Q = BE \oplus B'(A \oplus C)$ ,  $R = B'E \oplus B(A \oplus C)$ ,  $S = B \oplus B'E \oplus B(A \oplus C)$ ,  $T = B \oplus B'E \oplus B(A \oplus C) \oplus (A \oplus D)$  and  $U = B \oplus F$  the quantum cost of the NKHD gate is equal to  $QC = 11$  and its Hardware complexity is equal to  $HC = 6\alpha + 4\beta + 1\delta$  [10]

9) *TR Gate* : A reversible gate  $3 * 3$  having for inputs A, B and C as outputs  $P = A$ ,  $Q = A \oplus B$ ,  $R = AB' \oplus C$ ,  $S = AB \oplus C$  *bigoplus* D the quantum cost of the TR gate is equal to  $QC = 4$  and its Hardware complexity is equal to  $HC = 2\alpha + 1\beta + 1\delta$  [20]

10) *DVSM Gate* : A reversible gate  $4 * 4$  having for inputs A, B, C and D as outputs  $P = AB \oplus A'C$ ,  $Q = AB' \oplus A'C$ ,  $R = A'B \oplus AC$  and  $S = D \oplus AC \oplus A'B'$  the quantum cost of the TR gate is equal to  $QC = 11$  and its Hardware complexity is equal to  $HC = 5\alpha + 7\beta + 3\delta$  [11]

11) *MFRG1 Gate* : A reversible gate  $3 * 3$  having for inputs A, B and C as outputs  $P = A$ ,  $Q = A'B \oplus AC'$ ,  $R = A'C \oplus AB$ , the quantum cost of the TR gate is equal to  $QC = 4$  and its Hardware complexity is equal to  $HC = 2\alpha + 4\beta + 2\delta$  [12]

12) *MFRG2 Gate* : A reversible gate  $3 * 3$  having for inputs A, B and C as outputs  $P = A'$ ,  $Q = A'B \oplus AC$ ,  $R = A'C \oplus AB$ , the quantum cost of the TR gate is equal to  $QC = 4$  and its Hardware complexity is equal to  $HC = 2\alpha + 4\beta + 1\delta$  [12]

13) *OM Gate* : A reversible gate  $3 * 3$  having for inputs A, B and C as outputs  $P = A$ ,  $Q = AB \oplus C'$ ,  $R = A'B \oplus C'$ , the quantum cost of the OM gate is not mentioned in the literature and its hardware complexity is  $HC = 2\alpha + 2\beta + 2\delta$  [13]

14) *SOM Gate* : A reversible gate  $4 * 4$  having for inputs A, B, C and D as outputs  $P = AB \oplus C \oplus D$ ,  $Q = AB' \oplus C$ ,  $R = A'B \oplus C \oplus D$   $S = A'B' \oplus C \oplus D$ , the quantum cost of the SOM gate is not mentioned in the literature and its hardware complexity is  $HC = 5\alpha + 4\beta + 2\delta$  [13]

15) *UM Gate* : A reversible gate  $6 * 6$  having for inputs A, B, C, D, E and F as outputs  $P = A$ ,  $Q = AB \oplus C'$ ,  $R = A'B \oplus C'$   $S = A \oplus D$ ,  $T = DE \oplus F'$  and  $U = D'E \oplus F'$  the quantum cost of the SOM gate is not mentioned in the literature and its hardware complexity is  $HC = 5\alpha + 4\beta + 4\delta$  [13]

16) *RD Gate* : A reversible gate  $4 * 4$  having for inputs A, B, C and D as outputs  $P = AB \oplus D$ ,  $Q = (A+B)' \oplus D$ ,  $R = (A+B') \oplus C \oplus D$   $S = AB' \oplus D$ , the quantum cost of the RD gate is 8 and its hardware complexity is  $HC = 5\alpha + 2\beta + 2\delta$

### III. RELATED WORK

In this section, we will present the recent studies of the decoder design :

#### A. Decoder 2 to 4

1) *Design1 & Design2*: In 2020 Gunajit Kalita [13] proposed 2 decoders designs 2 to 4 as shown in Fig. 1 and 2, respectively .

\* Design1: The author has used the reversible gate SOM by assigning to the third and fourth input the value 0 so we have CG = 1, NGO = 0, NCI = 2, QC = not mentioned and HC =  $5\alpha + 4\beta + 2\delta$

\* Design2 : The author has used the reversible gate Um by assigning the third and the sixth input the value 1 and at the fourth input the value A and at the fifth input the value B 'so we have CG = 1, NGO = 2, NCI = 4, QC = not mentioned and HC =  $6\alpha + 4\beta + 4\delta$

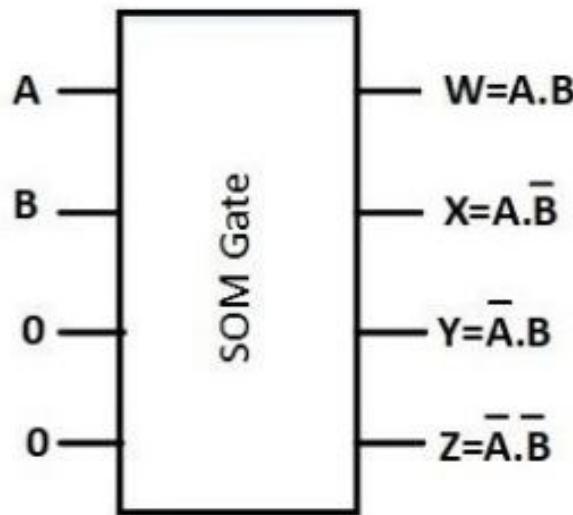


Fig. 1. Design used SOM Reversible Gate.

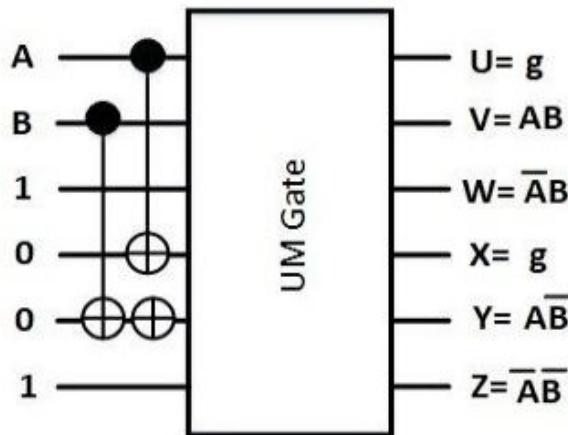


Fig. 2. Design used UM Reversible Gate.

2) *Design3 and Design4:* In 2013 Lafifa Jamal[9] proposed 2 decoder designs 2 to 4 as shown in Fig. 3 and 4, respectively .

\* Design 3: The author has used 1 reversible gate FG and 2 reversible gates FRG so we have CG = 3, NGO = 1, NCI = 3, QC = 11 and HC = $5\alpha + 8\beta + 2\delta$

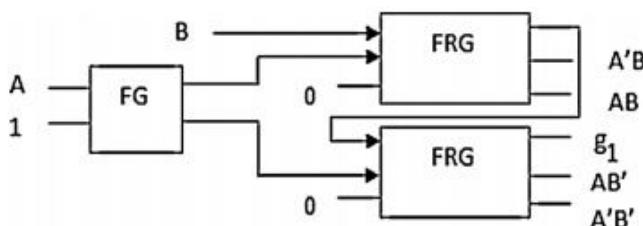


Fig. 3. Design used FG and 2 FRG Reversible Gates.

\* Design4: The author has used 1 reversible gate HL so we have CG = 1, NGO = 0, NCI = 2, QC = 7 and HC = $7\alpha + 9\beta + 3\delta$

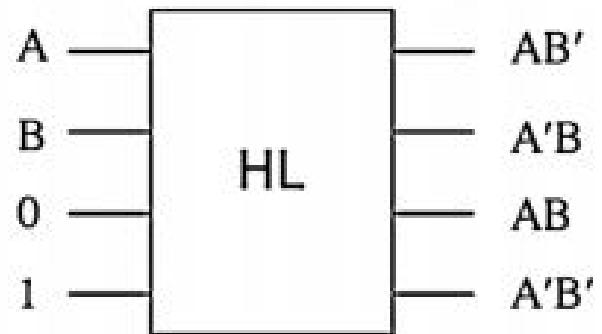


Fig. 4. Design used HL Reversible Gate.

3) *Design5:* In 2012 Ravish Aradhya HV [14]proposed 1 decoder designs 2 to 4 as shown in Fig. 5 by using 3 reversible gates of the FRG concerning its performance criteria we have CG = 3, NGO = 2, NCI = 3, QC = 15 and HC=6  $\alpha + 24\beta + 3\delta$

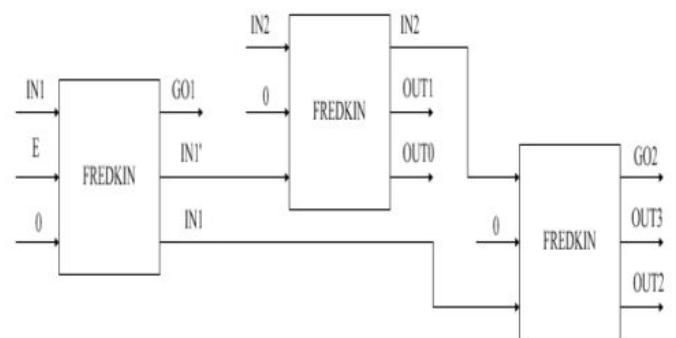


Fig. 5. Design used 3 FRG Reversible Gates.

4) *Design6:* In 2017 Nazma Tara [10] proposed 1 design of decoder 2 to 4 as shown in Fig. 6. by using 1 reversible gate of the NKHD by assigning to the third input the value 1 and to the fourth, fifth and sixth input the value 0 and concerning its performance criteria we have CG = 1, NGO = 2, NCI = 4, QC = 11 and HC = $6\alpha + 4\beta + 1\delta$

5) *Design7:* In 2018 Vandana Shukla [11]proposed 1 design of decoder 2 to 4 as shown in Fig. 7. by using 1 reversible gate of the DVSM by assigning to the third and the fourth input the value 0 and concerning its performance criteria we have CG = 1, NGO = 0, NCI = 2, QC = 11 and HC = $5\alpha + 7\beta + 3\delta$

6) *Design8:* In 2018 G. Greekanth [15] proposed 1 design of decoder 2 to 4 as shown in Fig. 8. by using 2 reversible NOT gates, 2 reversible gates RI by assigning to the 2 third inputs for each the value 0 and concerning its performance criteria we have CG = 2, NGO = 2, NCI = 2, QC = 8 and HC = $2\alpha + 6\beta + 4\delta$

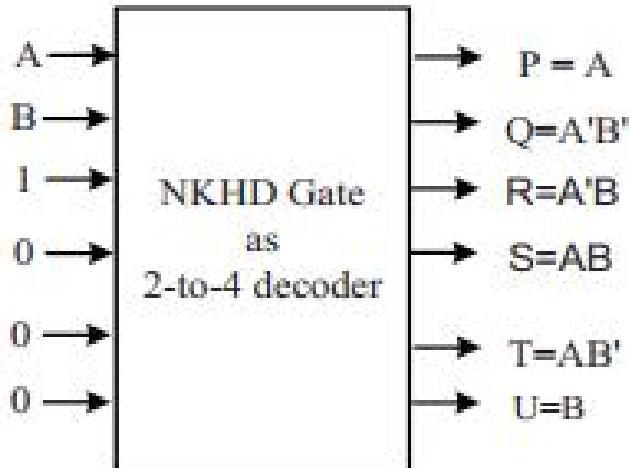


Fig. 6. Design used NKHD Reversible Gate.

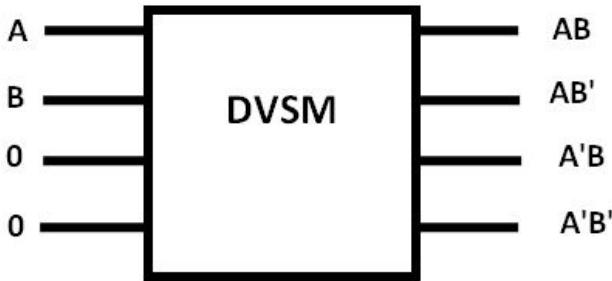


Fig. 7. Design used DVSM Reversible Gate.

7) *Design9*: In 2012 Md. Selim Al Mamun [12] proposed a design of decoder 2 to 4 as shown in Fig. 9 by using 1 reversible gate FG and 2 reversible gates MFRG1 whose performance criteria are as follows: CG = 3, NGO = 1, NCI = 3, QC = 9 and HC =  $5\alpha + 8\beta + 4\delta$

8) *Design10*: In 2017 Gopi Chand Naguboina [16] proposed a design of decoder 2 to 4 as shown in Fig. 10 by using 3 reversible gate CNOT, 1 reversible NOT gate, 1 reversible gate PG and 1 reversible gate TR whose performance criteria are as follows: CG = 6, NGO = 3, NCI = 3, QC = 11 and HC =  $7\alpha + 2\beta + 2\delta$

9) *Design11*: In 2019 Heranmoy Maity [17] proposed a design of decoder 2 to 4 as shown in Fig. 11 by using 1 reversible gate PG, whose performance criteria are as follows: CG = 1, NGO = 0, NCI = 2, QC = 9 and HC =  $7\alpha + 1\beta$

10) *Design12*: In 2013 Md. Shamsujjoha [18] proposed a design of decoder 2 to 4 as shown in Fig. 12 by using 1 reversible gate F2G and 2 reversible gates FRG whose performance criteria are as follows: CG = 3, NGO = 2, NCI = 4, QC = 12 and HC =  $6\alpha + 8\beta + 2\delta$

In the following we expose the recent designs of the 3 to 8 decoder:

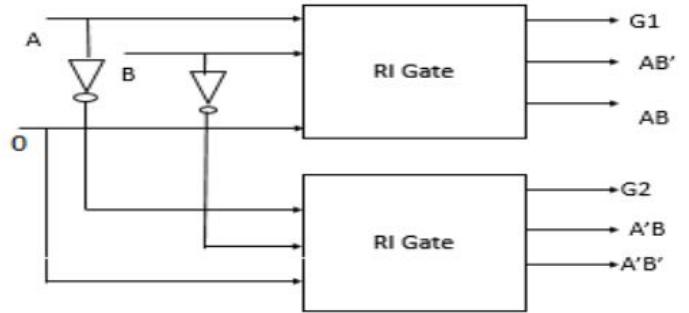


Fig. 8. Design used 2 RI Reversible Gate.

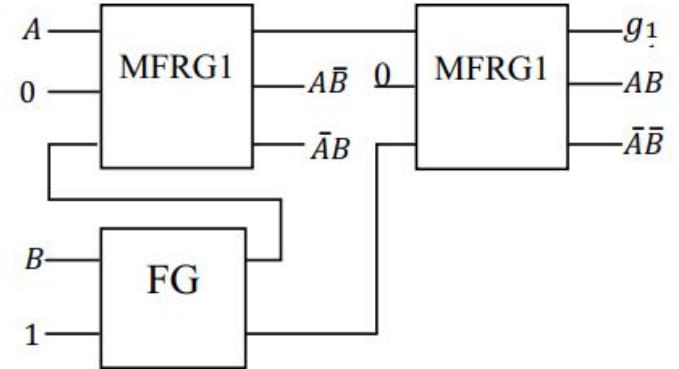


Fig. 9. Design used FG and 2 MFRG1 Reversible Gates.

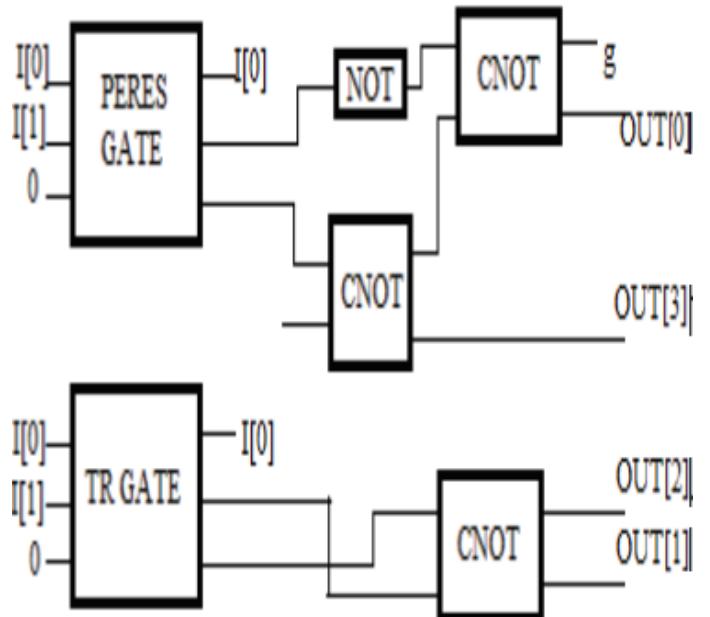


Fig. 10. Design used 3 Reversible Gate CNOT, 1 Reversible NOT Gate, 1 Reversible Gate PG and 1 Reversible Gate TR.

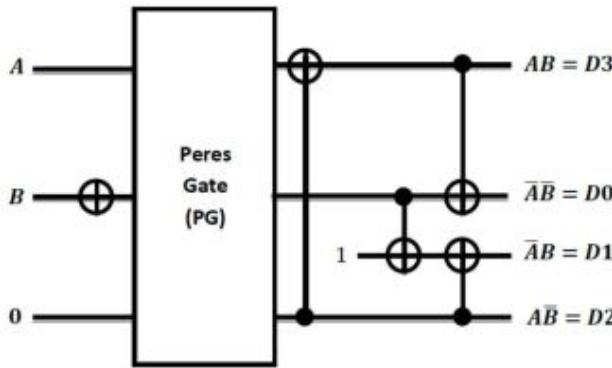


Fig. 11. Design used 1 PG Reversible Gate.

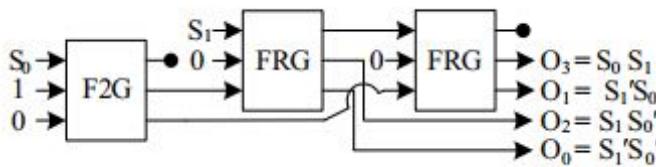


Fig. 12. Design used 1 F2G and 2 FRG Reversible Gates.

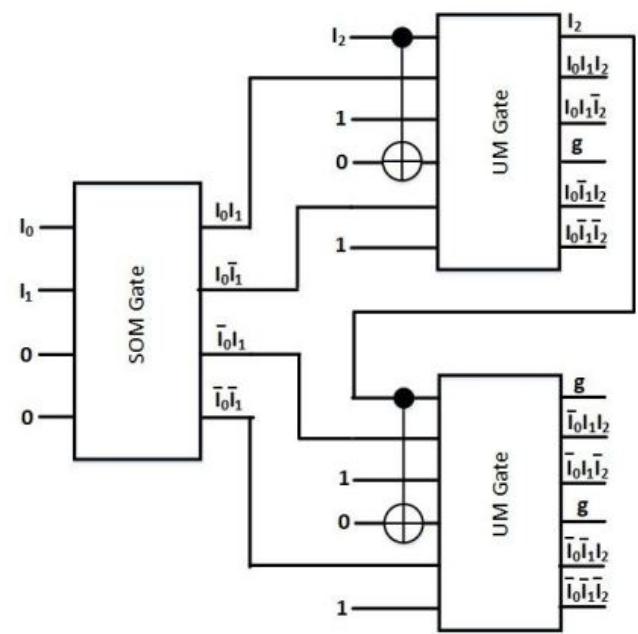


Fig. 13. Design used 1 SOM and 2 UM Reversible Gates.

### B. Decoder 3to8

1) *Design1 & Design2*: In 2020 Gunajit Kalita [13] proposed 2 decoders designs 3 to 8

\* design1 : The author has used 1 reversible gate SOM by assigning to the third and fourth input the value 0 and 2 reversible gates UM each of which by assigning to the third and sixth input the value 1 its performance criteria are as follows: CG = 3, NGO = 3, NCI = 8, QC = not mentioned in the literature and HC =  $17\alpha + 12\beta + 10\delta$  taking into account the 2 CNOT used as shown in Fig. 13.

\* design2 : The author had used 1 reversible gate SOM by assigning to the third and fourth input the value 0 and 4 reversible gates OM each of which by assigning to the third input the value 1 its performance criteria are as follows: CG = 5, NGO = 1, NCI = 6, QC = not mentioned in the literature and HC =  $13\alpha + 12\beta + 10\delta$  as shown in Fig. 14.

2) *Design3 & Design4*: In 2013 Lafifa Jamal[9] proposed 2 decoder designs 3 to 8

\* design 3 : The author has used 1 reversible gate FG by assigning the second input the value 1 and the rest of 6 reversible gates FRG by assigning the third input the value 0 so we have CG = 7, NGO = 2, NCI = 7, QC = 31 and HC =  $13\alpha + 24\beta + 6\delta$  as shown in Fig. 15.

The 2 to 4 reversible decoder circuit is equivalent to fig3

\* design4 : Using 1 reversible gate HL by assigning the third input the value 0 and the fourth input the value 1 and the rest of 4 reversible gates FRG by assigning the third input the value 0 so we have CG = 5, NGO = 1, NCI = 6, QC = 27 and HC =  $15\alpha + 25\beta + 7\delta$  as shown in Fig. 16.

The 2 to 4 reversible decoder circuit is equivalent to fig4.

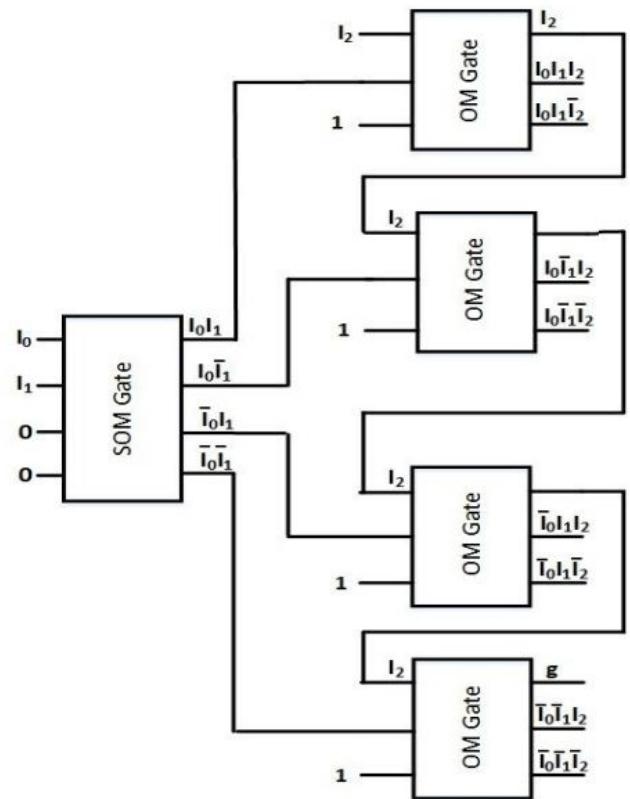


Fig. 14. Design used 1 SOM and 4 OM Reversible Gates.

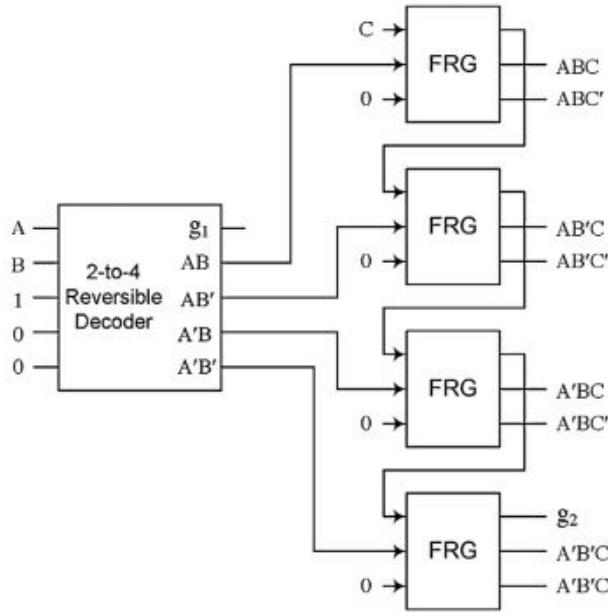


Fig. 15. Design used 1 FG and 6 FRG Reversible Gates.

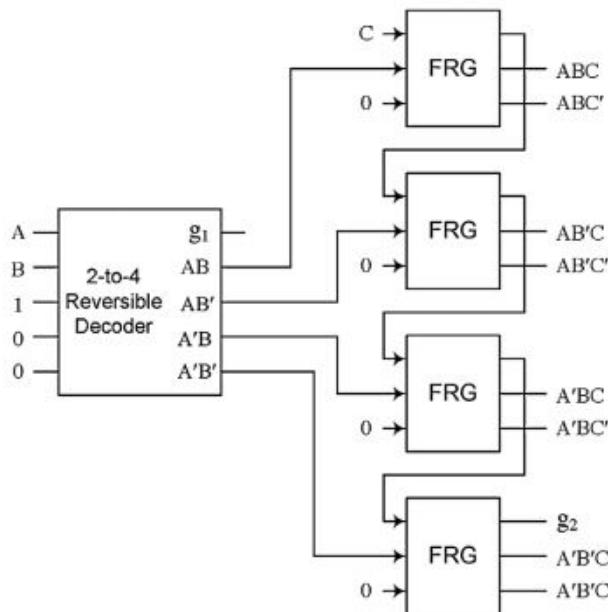


Fig. 16. Design used 1 HL and 4 FRG Reversible Gates.

*3) Design5:* In 2012 Ravish Aradhya HV [14] proposed 1 decoder designs 3 to 8 by using 7 reversible gates of the FRG, concerning one reversible FRG gate by assigning its second input to the value 1 and the third input to the value 0 and for the rest of the 6 FRG reversible gates, the value 0 is assigned to the third input by concerning its performance criteria we have CG = 7, NGO = 2, NCI = 8, QC = 35 and HC=14  $\alpha + 28\beta + 7\delta$  as shown in Fig. 17.

*4) Design6:* In 2017 Nazma Tara [10]proposed a design of the decoder 3 to 8 using an NKHD reversible gate by assigning

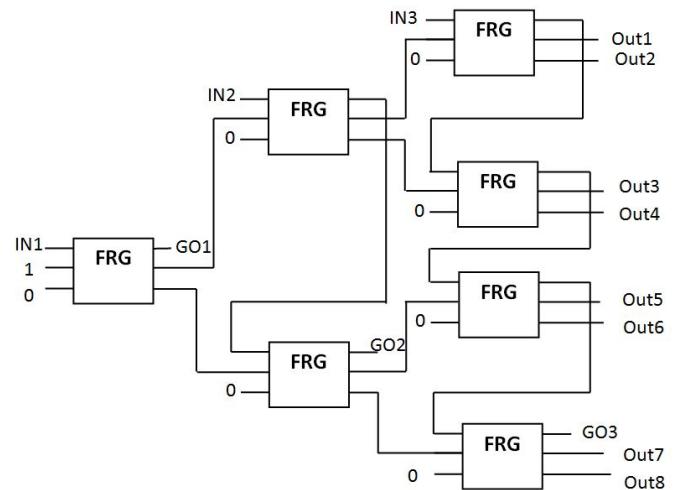


Fig. 17. Design used 7 FRG Reversible Gates.

to the third input the value 1 and to the fourth, fifth and sixth input the value 0 and 4 FRG reversible gates assigning to the third input for each the value 0 concerning its performance criteria we have CG = 5, NGO = 3, NCI = 8, QC = 31 and HC=14  $\alpha + 20\beta + 5\delta$  as shown in Fig. 18.

Fig. 18 shows the 2 to 4 reversible decoder circuit equivalent design shown in Fig. 6.

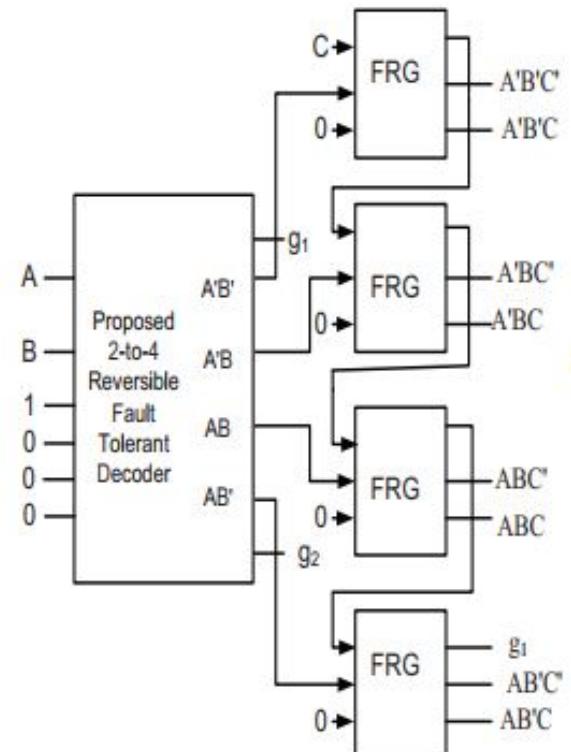


Fig. 18. Design used 7 FRG Reversible Gates.

5) *Design7*: In 2018 Vandana Shukla [11] proposed a design of the decoder 3 to 8 using an DVSM reversible gate by assigning to the third and the fourth input the value 1 and for 4 FRG reversible gates assigning to the third input for each the value 0 concerning its performance criteria we have CG = 5, NGO = 1, NCI = 6, QC = 31 and HC=13  $\alpha + 23\beta+7\delta$  as shown in Fig. 19.

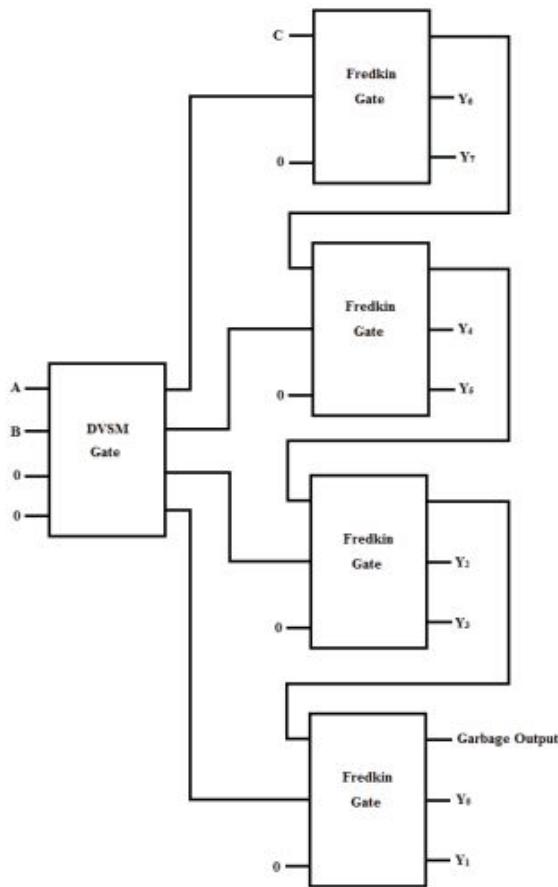


Fig. 19. Design used DVSM and 4 FRG Reversible Gates.

6) *Design8*: In 2018 G.Sreekanth [15] proposed a design of the decoder 3 to 8 using 6 RI reversible gate by assigning to the third input the value 0 for all gates concerning its performance criteria we have CG = 6, NGO = 3, NCI = 6, QC = 24 and HC=6  $\alpha + 18\beta+8\delta$  as shown in Fig. 20. taking into account 2 NOT used

The 2 to 4 reversible decoder circuit is equivalent to Fig. 8.

7) *Design9*: in 2012 Md. Selim Al Mamun [12]proposed a design of decoder 3 to 8 using 1 reversible gate FG and 2 reversible gates MFRG1 and 4 reversible MFGR2 by assigning to the third input the value 0 , whose performance criteria are as follows: CG = 7, NGO = 2, NCI = 7, QC = 29 and HC = 13 $\alpha + 24\beta+9\delta$  as shown in Fig. 21.

The 2 to 4 reversible decoder circuit is equivalent to Fig. 9.

8) *Design10*: In 2016 Anish Kumar Saha [19] proposed a design of decoder 3 to 8 whose performance criteria are as

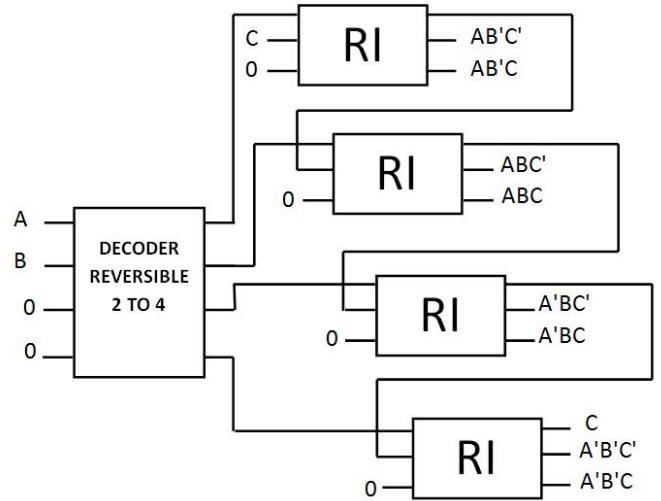


Fig. 20. Design used 6 RI Reversible Gates.

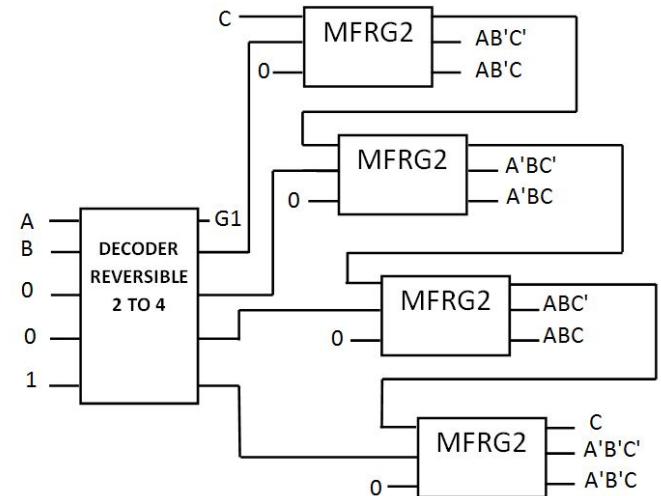


Fig. 21. Design used 1FG 2 MFRG1 and 4 MFRG2.

follows: CG = 10, NGO = 3, NCI = 8, QC = 50.

9) *Design11*: (fig20) in 2017 Gopi Chand Naguboina[16] proposed a design of decoder 2 to 4 using 3 reversible gate FG, 1 reversible NOT gate, 1 reversible gate PG and 1 reversible gate TR and 4 FRG reversible by assigning to the second input the value 0 gates whose performance criteria are as follows: CG = 10, NGO = 3 , NCI = 7, QC = 31 and HC = 15 $\alpha + 18\beta+6\delta$  as shown in Fig. 22.

10) *Design12*: In 2013 Md. Shamsujjoha [18] proposed a design of decoder 3 to 8 using 1 F2G reversible gate and 6 FRG reversible gate, by assigning to the second input the value 0 gates whose performance criteria are as follows: CG = 10, NGO = 7 , NCI = 8, QC = 32 and HC = 14 $\alpha + 24\beta+6\delta$  as shown in Fig. 23.

### C. Decoder $n$ to $2^n$

1) *Design1 & Design2*: In 2020 Gunajit Kalita [13]proposed 2 decoders designs n to  $2^n$

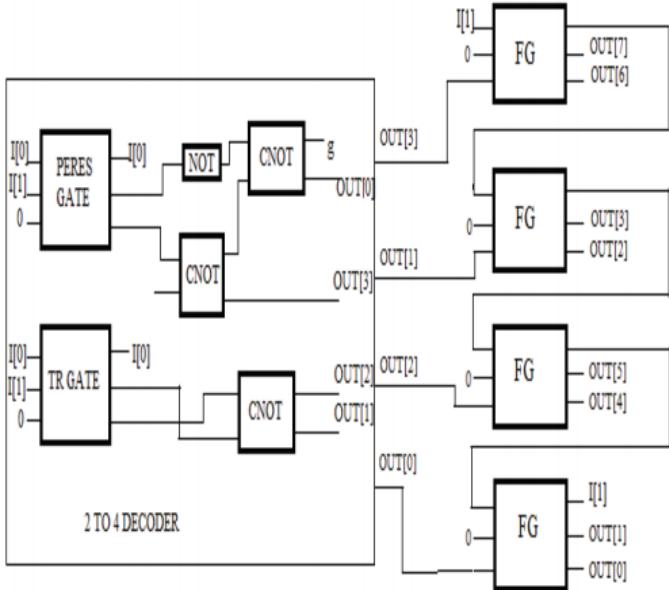


Fig. 22. Design used 3 Reversible Gate CNOT, 1 Reversible NOT Gate, 1 Reversible Gate PG 1 Reversible Gate TR and 4 FRG.

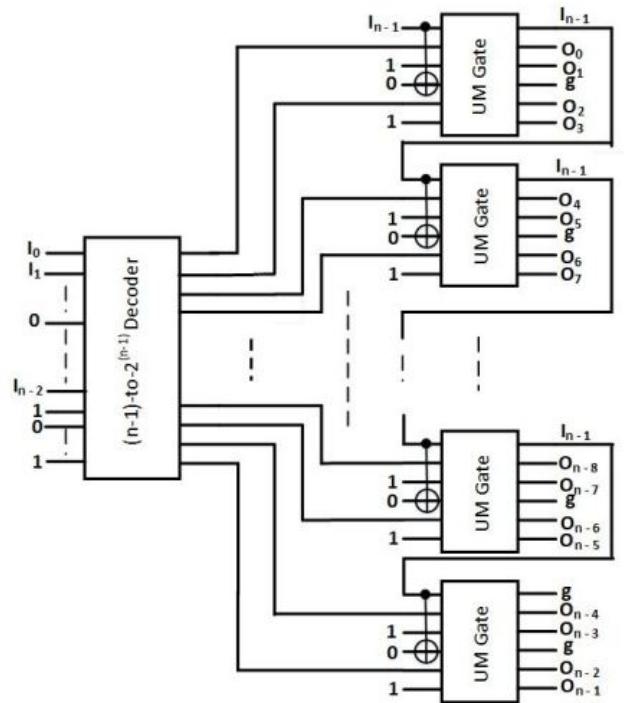


Fig. 24. Design Decoder n to  $2^n$  used SOM and UM.

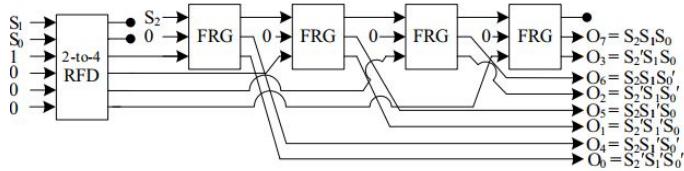


Fig. 23. Design used 1 f2G and 6FRG.

\* design1 : To build the circuit of the decoder  $n$  to  $2^n$  he used a reversible gate SOM and 2 reversible gates UM and assigning to each increment 2 reversible gates Um to each reversible gate UM previous as shown in Fig. 24.

Concerning the performance criteria we have  $CG = (2^{n-1} - 1)$ ,  $NGO = (2^{n-1} + n - 4)$ ,  $NCI = 32^{n-1} - 4$ , QC not mentioned in the literature and  $HC = HC(SOM) + (2^{n-1} - 2) HC(UM)$  so  $HC = (52^{n-1} - 5)\alpha + (42^{n-1} - 4)\beta + (42^{n-1} - 6)\delta$  taking into account the  $2^{n-2}$  CNOT at each level of  $n$

\* design2 : To build the circuit of the decoder  $n$  to  $2^n$  he used a reversible gate SOM and 4 reversible gates OM and assigning to each increment 2 reversible gates Um to each reversible gate OM previous as shown in Fig. 25. Concerning the performance criteria we have  $CG = (2^n) - 3$ ,  $NGO = (n - 2)$ ,  $NCI = 2^{n-2}$ , QC not mentioned in the literature and  $HC = HC(SOM) + (2^n - 4) HC(OM)$  so  $HC = (2^{n+1} - 3)\alpha + (2^{n+1} - 4)\beta + (2^{n+1} - 6)\delta$

2) Design3 & Design4: In 2013 Lafifa Jamal[9] proposed 2 decoder designs  $n$  to  $2^n$

\* design 3 : To build the circuit of the decoder  $n$  to  $2^n$  he used 1 reversible gate FG and 2 reversible gates FRG and assigning to each increment 2 reversible gates FRG to each reversible gate FRG previous as shown in Fig. 26.

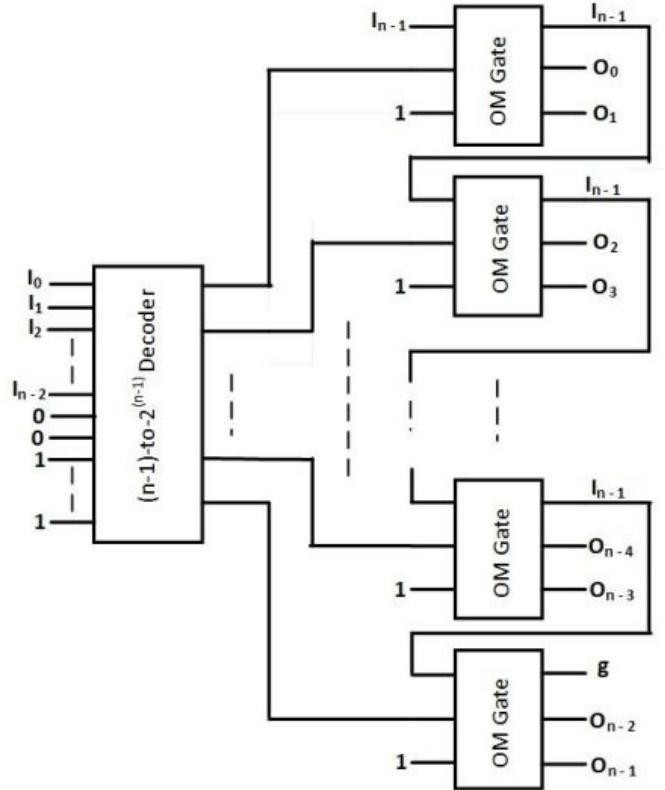


Fig. 25. Design Decoder n to  $2^n$  used SOM and OM.

Concerning the performance criteria we have  $CG = (2^n) - 1$ ,  $NGO = (n-1)$ ,  $NCI = 2^n - 1$ ,  $QC = 5 \cdot 2^{n-9}$  and  $HC = HC$  ( $FG + 2FRG$ ) +  $(2^n - 4) HC$  ( $FRG$ ) =  $HC = (2^n + 1 - 3)\alpha + (2^n + 2 - 8)\beta + (2^n - 2)\delta$

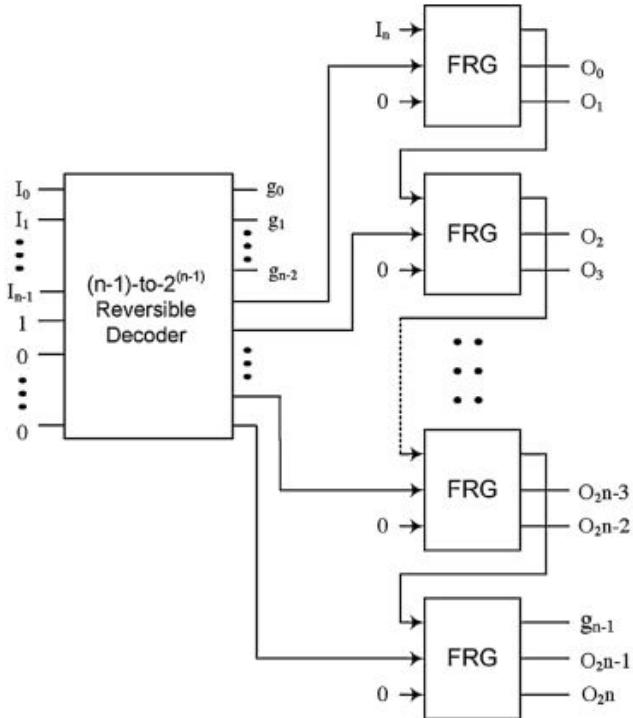


Fig. 26. Design Decoder  $n$  to  $2^n$  used FG and FRG.

\* design4: To build the circuit of the decoder  $n$  to  $2^n$  he used 1 reversible gate HL and 4 reversible gates FRG and assigning to each increment 2 reversible gates FRG to each reversible gate FRG previous as shown in Fig. 27.

Concerning the performance criteria we have  $CG = (2^n) - 3$ ,  $NGO = (n-2)$ ,  $NCI = 2^n - 2$ ,  $QC = 5 \cdot 2^{n-13}$  and  $HC = HC$  (HL) +  $(2^n - 4) HC$  ( $FRG$ ) =  $HC = (2^n + 7)\alpha + (2^{n+1} + 9)\beta + (2^{n-1} + 3)\delta$

3) Design5: In 2012 Ravish Aradhya HV [14] proposed a decoder designs  $n$  to  $2^n$  used 3 reversible gate FRG and assigning to each increment 2 reversible gates FRG to each reversible gate FRG previous as shown in Fig. 28.

Concerning the performance criteria we have  $CG = (2^n) - 1$ ,  $NGO = (n)$ ,  $NCI = 2^n$ ,  $QC = 5 \cdot 2^{n-5}$  and  $HC = HC$  (3FRG) +  $(2^n - 4) HC$  ( $FRG$ ) =  $HC = (2^{n+1} - 2)\alpha + (2^{n+2} - 4)\beta + (2^n - 1)\delta$

4) Design6: In 2017 Nazma Tara [10] proposed a decoder designs  $n$  to  $2^n$  used 1 reversible gate NKHD and 2 reversible gates FRG and assigning to each increment 2 reversible gates FRG to each reversible gate FRG previous as shown in Fig. 29.

Concerning the performance criteria we have  $CG = (2^n) - 3$ ,  $NGO = n$ ,  $NCI = 2^n$ ,  $QC = 5 \cdot 2^{n-9}$  and  $HC = HC$  (NKHD) +  $(2(n) - 4) HC$  ( $FRG$ ) =  $HC = (2^{n+1} - 2)\alpha + (2^{n+2} - 12)\beta + (2^n - 3)\delta$

5) Design7: In 2012 Md. Selim Al Mamun [12] a decoder designs  $n$  to  $2^n$  used 1 reversible gate FG ,2 reversible gates MFRG1 and 2 reversible gates MFRG2 and assigning to each

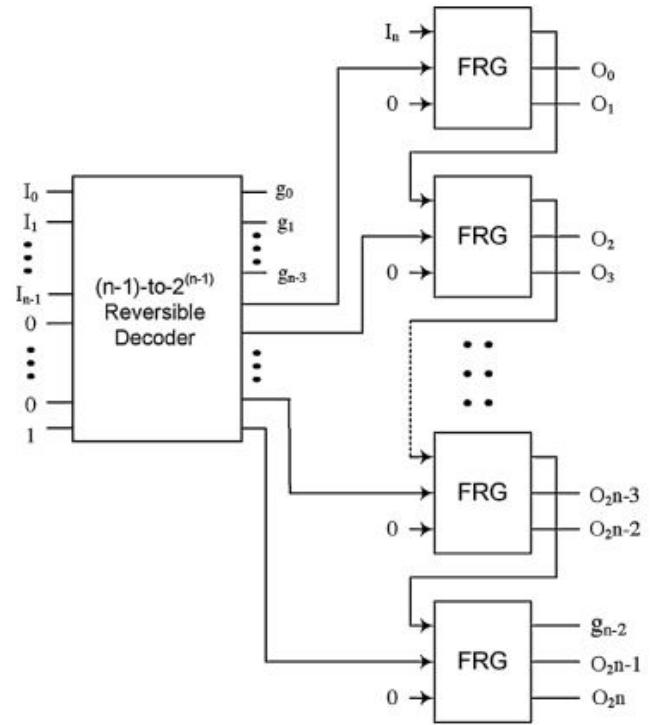


Fig. 27. Design Decoder  $n$  to  $2^n$  used HL and FRG.

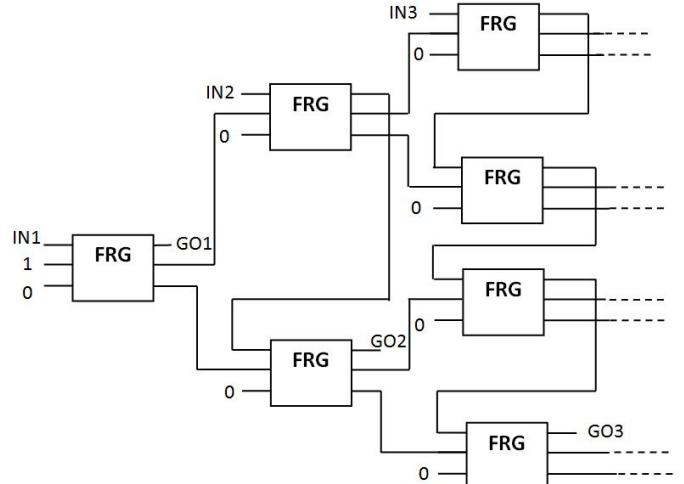


Fig. 28. Design Decoder  $n$  to  $2^n$  using FRG.

increment 2 reversible gates MFRG2 to each reversible gate MFRG2 previous.

Concerning the performance criteria we have  $CG = (2^n) - 1$   $NGO = n - 1$ ,  $NCI = 2^{n-1}$ ,  $QC = 5 \cdot 2^{n-11}$  and  $HC = HC$  (2MFRG1+FG) +  $(2^n - 4) HC$  (MFRG2) =  $HC = (2^{n+1} - 3)\alpha + (2^{n+2} - 8)\beta + 2^n\delta$

6) Design8: In 2016 Anish Kumar[19] proposed a decoder designs  $n$  to  $2^n$  concerning the performance criteria we have  $CG = 10$ ,  $NGO = n$ ,  $NCI = 2^n$ ,  $QC = 6 \cdot 2^n$  and  $HC =$  not mentioned in the literature.

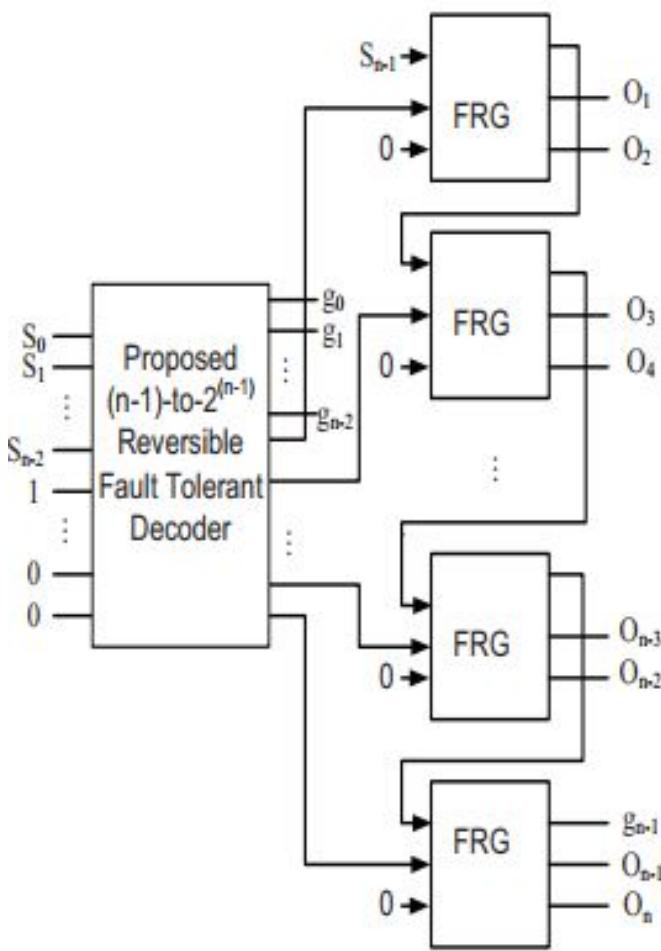


Fig. 29. Design Decoder  $n$  to  $2^n$  used NKHD and FRG.

7) *Design9:* In 2013 Md. Shamsujjoha [18] proposed  $n$  to  $2^n$  using 1 F2G reversible gate and 2 reversible gates FRG ,and assigning to each increment 2 reversible gates FRG to each reversible gate FRG previous as shown in Fig. 30. Concerning the performance criteria we have  $CG = (2^n)-1$   $NGO = n$ ,  $NCI = 2^n$  , $QC = 52^n - 8$  and  $HC = HC(F2G) + (2^n-2)HC(FRG) = HC = (2^{n+1}-2)\alpha + (2^{n+2}-8)\beta + (2^n-2)\delta$

**Limitations of previous studies:** We find in these previous studies a certain limitation in terms of less optimized performance criteria, the evidence is that we were able to make our designs with better performance criteria than the previous works while keeping the same functionality.

#### IV. OUR PROPOSED DESIGN OF DECODER 2 TO 4, 3 TO 8 AND N TO $2^n$

In this paragraph we will present our circuits concerning the decoder 2 to 4, 3 to 8 and  $n$  to  $2^n$

Our work is based on the article [13] ,we try to modify it to improve certain performance criteria, starting with:

##### A. Decoder 2 to 4

We thought of exploiting its circuit 2 to 4 [13] by replacing the reversible gate SOM by that of the RD and to assign to the third and fourth input the value 0 Fig. 31 shows our design of decoder 2 to 4.

Concerning the performance criteria of our design we have  $CG=1$ ,  $NGO=0$  , $NCI=2$ ,  $QC=8$  et  $HC= 5\alpha + 2\beta + 2\delta$

##### B. Decoder 3 to 8

After using the decoder circuit 3 to 8 of the [13], the reversible gate SOM has also been replaced by that of the RD, and the 2 reversible gates UM by 4 reversible gates RI.

Fig. 32 shows our design of decoder 3 to 8.

The performance criteria obtained are as follows:  $CG=5$ ,  $NGO=1$ ,  $NCI=6$  , $QC=24$  and  $HC=9\alpha + 14\beta + 6\delta$

##### C. Decoder $n$ to $2^n$

Our conception of decoding  $n$  to  $2^n$  is done by adopting our decoder circuit 3 to 8 by adding to each reversible gate RI 2 reversible gates RI. Fig. 33 shows our design of the decoder  $n$  to  $2^n$ .

The performance criteria obtained are as follows:

Concerning the performance criteria we have as follows:

1) *lemma 1:*  $CG = 2^n - 3$

**Proof:** we will demonstrate it recurrently for  $n = 2$  we have  $CG = 2^2 - 3 = 4 - 3 = 1$  that's correct because we have only one reversible gate which is RD.

Suppose that for  $n-1$  we have  $CG = 2^{n-1} - 3$  and prove for  $n$  we have  $CG = 2^n - 3$

for  $n$  on  $CG = 2^{n-1} - 3 + 2^{n-1}$  because the  $n$  th column of the reversible gates RI we have in total  $2^n - 1$  therefore  $CG = 2 * 2^{n-1} - 3 = 2^n - 3$  so it's correct then  $CG = 2^n - 3$

2) *lemma 2:* \*  $NGO = n - 2$

**Proof:** we will demonstrate it recurrently for  $n = 2$  we have  $NGO = 2 - 2 = 0$  that's correct because the RD reversible gate has no garbage output.

Suppose that for  $n-1$  we have  $NGO = n - 2 = n - 3$  and prove for  $n$  we have  $NGO = n - 2$  for  $n$  on  $NGO = n - 3 + 1 = n - 2$  because at the  $n$  th column of the RI reversible gates there is only one garbage output so it's correct then  $NGO = n - 2$

3) *lemma 3:* \*  $NCI = 2^{n-2}$

**Proof:** we will demonstrate it recurrently for  $n = 2$  we have  $NCI = 2^2 - 2 = 2$  that's correct because the RD reversible gate has 2 constants inputs.

Suppose that for  $n-1$  we have  $NCI = 2^{n-1} - 2$  and prove for  $n$  we have  $NCI = 2^n - 2$  for  $n$  on  $NCI = 2^{n-1} - 2 + 2^{n-1} = 2^n - 2$  because at the  $n$  th column of the RI reversible gates there we have  $2^{n-1}$  so it's correct then  $NCI = 2^n - 2$

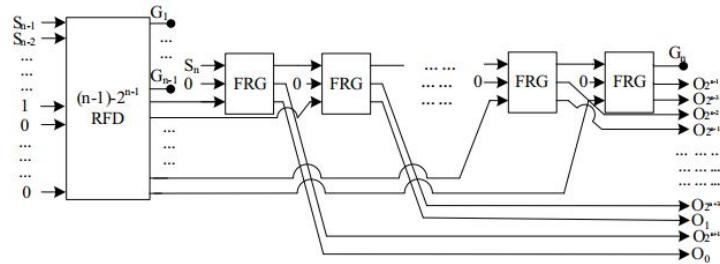


Fig. 30. Design Decoder  $n$  to  $2^n$  used F2G and FRG.

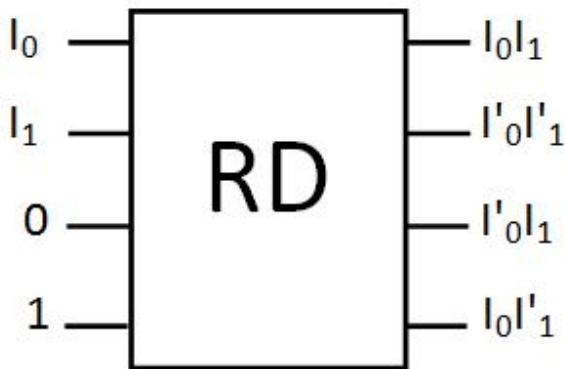


Fig. 31. Our Decoder Design 2 to 4.

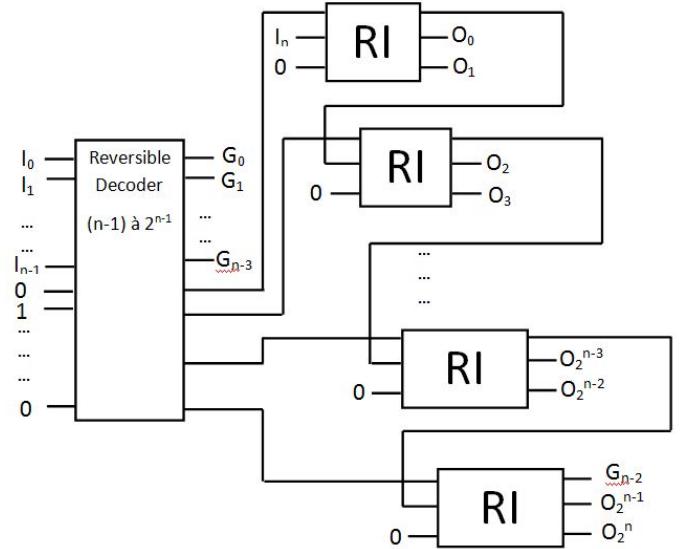


Fig. 33. Our Decoder Design  $n$  to  $2^n$ .

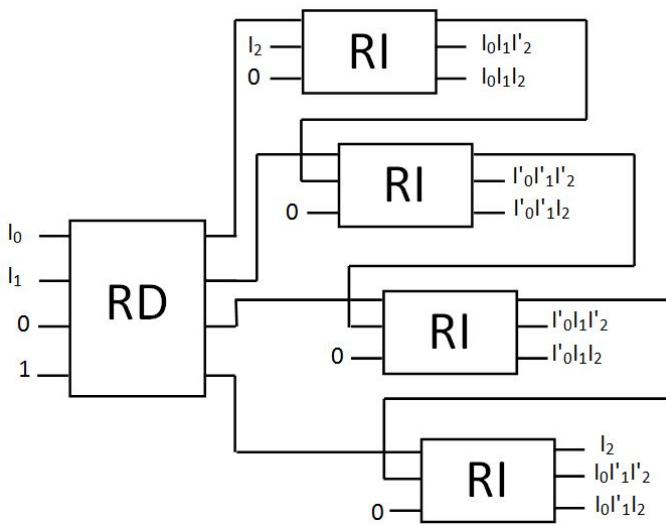


Fig. 32. Our Decoder Design 3 to 8.

4) lemma 4: \*  $QC = 4 (2^n - 2)$

**Proof:** we will demonstrate it recurrently for  $n = 2$  we have  $CG = 4 * (2^2 - 2) = 4 * (4 - 2) = 8$  that's right because the quantum cost of the reversible gate RD is 8.

Suppose that for  $n-1$  we have  $QC = 4 (2^{n-1} - 2)$  and prove for  $n$  we have  $QC = 4 (2^n - 2)$

for  $n$  on  $QC = 4 (2^{n-1} - 2) + 4 * 2^{n-1}$  because at the  $n$  th column of the reversible gates RI we have in total  $2^{n-1}$  reversible gates that we must multiply by 4 to have the quantum cost of the  $n$  th column so  $QC = 4 (2^{n-1} - 2) + 4 * 2^{n-1} = 4 (2^n - 2)$  so it's correct then  $QC = 4 (2^n - 2)$ .

5) lemma 5: \*  $HC = HC = 5\alpha + 2\beta + 2\delta + 2^{n-1}(1\alpha + 3\beta + 1\delta) = (2^{n-1} + 5)\alpha + (3 * 2^{n-1} + 2)\beta + (2^{n-1} + 2)\delta$

**Proof:** In our design of the decoder  $n$  to  $2^n$  we have a reversible gate RD and 2  $(n-1)$  reversible gates RI so we have

$$HC = HC(RD) + HC(2^{n-1} RI)$$

$$\begin{aligned} HC &= 5\alpha + 2\beta + 2\delta + 2^{n-1}(1\alpha + 3\beta + 1\delta) \\ &= (2^{n-1} + 5)\alpha + (3 * 2^{n-1} + 2)\beta + (2^{n-1} + 2)\delta \end{aligned}$$

## V. RESULT AND DISCUSSION

So in this paragraph we will compare our results obtained compared to recent studies of decoder 2 to 4, 3 to 8 and  $n$  to  $2^n$

#### A. Comparative Table of Decoder Performance Criteria 2 to 4, 3 to 8 and n to $2^n$

After proving the results obtained from decoders 2 to 4, 3 to 8 and  $n$  to  $2^n$  for our proposed designs and recent and exploited ones we can draw up the following tables showing the% improvement in performance criteria,starting with:

1) Comparative Table of Decoder Performance Criteria 2 to 4 : Table I shows the% improvement in performance criteria about decoder 2 to 4.

TABLE I. COMPARATIVE TABLE OF DECODER PERFORMANCE CRITERIA 2 TO 4

Decoder 2to4	CG	NGO	NCI	QC	HC
Our design	1	0	2	8	$5\alpha +2\beta+2\delta$
design1 [13]	1	0	2	—	$5\alpha +4\beta+2\delta$
Design2 [13]	1	2	4	—	$6\alpha +4\beta+4\delta$
Design3 [9]	3	1	3	11	$5\alpha +8\beta+2\delta$
Design4 [9]	1	0	2	7	$7\alpha +9\beta+3\delta$
[14]	3	2	3	15	$6\alpha +24\beta+3\delta$
[10]	1	2	4	11	$6\alpha +4\beta+1\delta$
[11]	1	0	2	11	$5\alpha +7\beta+3\delta$
[15]	2	2	2	8	$2\alpha +6\beta+4\delta$
[12]	3	1	3	9	$5\alpha +8\beta+4\delta$
[16]	6	3	3	11	$7\alpha +2\beta+2\delta$
[17]	1	0	2	9	$7\alpha +1\beta$
[18]	3	2	4	12	$6\alpha +8\beta+2\delta$
%Imp Design1 [13]	—	—	—	—	50% of AND
%Imp Design2 [13]	—	100	50	—	16.67 CNOT , 50 (AND,NOT)
%Imp Design3 [9]	66,67	100	33,33	27,27	75AND
%Imp Design4 [9]	—	—	—	—	28,57CNOT 77,78AND 33,33NOT
%Imp [14]	66,67	100	33,33	46,66	16,67CNOT 91,66AND 33,33NOT
%Imp [10]	—	100	50	27,27	16,67 CNOT 50AND
%Imp [11]	—	—	—	27,27	71,42AND 33,33NOT
%Imp [15]	50	100	—	—	66,67AND 50NOT
%Imp [12]	66,67	100	33,33	11,11	75AND 50NOT
%Imp [16]	83,33	100	33,33	27,27	28,57CNOT
%Imp [17]	—	—	—	11,11	28,57CNOT
%Imp [18]	66,67	100	50	33,33	16,67CNOT 75AND

Based on the results obtained in the recent table, we were able to reduce in terms of:

-Number of gates: 66.67 % compared to design3 [9], design [14], design [12] and design [18], 50 % compared to design [15] and 83.33 % compared to design [16].

-Number of garbage outputs: 100 % compared to design2 [13], design3 [9], design [14], design [10], design [15], design [12], design [16] and design [18].

-Number of constant inputs: 50 % compared to design2 [13], design [11] and design [18], 33.33 % compared to design3 [9], design [14], design [12] and design [16].

-Quantum cost: 27.27 % compared to design3 [9], design [10], design [11], design [16], 46.66 % compared to design [14].

-Hardware Complexity: \* number of CNOT gates: 16.67 % compared to design2 [13], [14] [10], [18], 28.75 % compared to design4 [9].

\* Number of AND gates: 50 % compared to design1 [13], design2 [13], [10], 75 % compared to design3 [9], [12], design

[18] 77.78 % compared to design4 [9], 91.66 % compared to design [14], 71.42 % compared to design [11] and 66.67 % compared to design [15]

\* Number of NOT gates: 50 % compared to design2 [13], 33.33 % compared to design4 [9], [14].

From these results we draw up our Table 3.10 based on which we can present the graph containing the performance criteria in the form of bars Fig. 34.

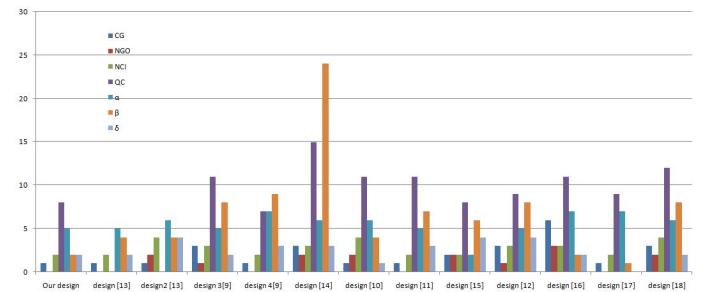


Fig. 34. Graph of Decoder Performance Criteria 2 to 4 of Recent Studies and our Design.

2) Comparative Table of Decoder Performance Criteria 3 to 8 : Table II shows the% improvement in performance criteria about decoder 3 to 8.

TABLE II. COMPARATIVE TABLE OF DECODER PERFORMANCE CRITERIA 3 TO 8

Decoder 3to8	CG	NGO	NCI	QC	HC
Our design	5	1	6	24	$9\alpha +14\beta+6\delta$
Design1[13]	3	3	8	—	$17\alpha +12\beta+10\delta$
Design2[13]	5	1	6	—	$13\alpha +12\beta+10\delta$
Design3[9]	7	2	7	31	$13\alpha +24\beta+6\delta$
Design4[9]	5	1	6	27	$15\alpha +25\beta+7\delta$
[14]	7	2	8	35	$14\alpha +28\beta+7\delta$
[10]	5	3	8	31	$14\alpha +20\beta+5\delta$
[11]	5	1	6	31	$13\alpha +23\beta+7\delta$
[15]	6	3	6	24	$6\alpha +18\beta+8\delta$
[12]	7	2	7	29	$13\alpha +24\beta+9\delta$
[19]	10	3	8	50	—
[16]	10	3	7	31	$15\alpha +18\beta+6\delta$
[18]	10	7	8	32	$14\alpha +24\beta+6\delta$
%Imp Design1[13]	—	66,67	25	—	47,05CNOT 40NOT
%Imp Design2[13]	—	—	—	—	30,76 CNOT 40NOT
%Imp Design3[9]	28,57	50	14,28	22,58	30,76CNOT 41,66AND
%Imp Design4[9]	—	—	—	11,11	40CNOT 44AND 14,28NOT
%Imp [14]	28,57	50	25	31,42	35,71CNOT 50AND 14,28NOT
%Imp [10]	—	66,67	25	22,58	35,71 CNOT 30AND
%Imp [11]	—	—	—	22,58	30,76CNOT 39,13AND 14,28NOT
%Imp [15]	16,67	66,67	—	—	22,22AND 25NOT
%Imp [12]	28,57	50	14,28	17,24	30,76 CNOT 41,66AND 33,33NOT
%Imp [19]	50	66,67	25	52	—
%Imp [16]	50	66,67	14,28	22,58	40CNOT 22,22AND
%Imp [18]	50	85,71	25	25	35,71CNOT 41,66AND

Based on the results obtained in the recent table, we were able to reduce in terms of:

-Number of gates: 28.57 % with respect to design3 [9], design [14], design [12], 50 % with respect to design [19], design [16], design [18] and 16, 67 % compared to design [15].

-Number of garbage outputs: 66.67 % compared to design1 [13], design [10], design [14], design [15], design [19], design [16] 50 % compared to design3 [9] design [14] design [12] and 85.71 % compared to design [18].

Number of constant inputs: 25 % with respect to design1 [13], design [14] design [10], design [19] and design [18], 14.28 % with respect to design3 [9], design [12] and design [16].

-Quantum cost: 22.58 % compared to design3 [9], design [10], design [11], design [16], 11.11 % compared to design4 [9] 31.42 % by with respect to design [14] 17.24 % with respect to design [12] 52 % with respect to design [19] and 25 % with respect to design [18].

-Hardware Complexity: \* number of CNOT gates: 47.05 % compared to design1 [13], 30.76 % compared to design2 [13] design3 [9] design [11], design [12], 35.71 % compared to design [14] design [10] design [18], 40 % compared to design [16].

\* Number of AND gates: 41.66 % compared to design3 [9], design [12], design [18], 44 % compared to design4 [9] 50 % compared to design [14], 30 % with respect to design [10], 39.13 % with respect to design [11] 22.22 % with respect to design [15] and design [16]

\* Number of gates NOT: 40 % compared to design1 [13], design2 [13] 14.28 % compared to design4 [9] 25 % compared to design [15], 33.33 % by in relation to design [12].

From these results we draw up our Table 3.11 based on which we can present the graph containing the performance criteria in the form of bars Fig. 35.

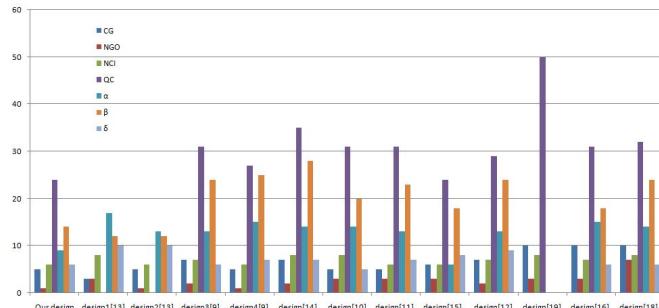


Fig. 35. Graph of Decoder Performance Criteria 3 to 8 of Recent Studies and Our Design.

\*

3) Comparative Table of Decoder Performance Criteria  $n$  to  $2^n$  : Table III shows the% improvement in performance criteria about decoder  $n$  to  $2^n$ .

Then this table represents the performance criteria of each design of decoder  $n$   $2^n$  and the % improvement in terms of these of our design compared to recent decoders, all of these parameters of which are expressed as a function of  $n$ .

In the column of % improvement of HC we represent respectively our percentages of CNOT, AND and NOT which are separated by the symbol -.

After having presented the improvements obtained from our design of the decoder  $n$  at  $2n$  in terms of performance criteria, we will assume that  $n$  tends to infinity in order to be

able to give improvements of % and therefore to obtain the following Table IV.

Then when  $n$  tends to infinity we obtain the following improvements according to each performance criteria:

-Number of garbage outputs: 100% compared to design 1 [13].

-Number of constant inputs: 33% compared to design 1 [13].

-Quantum cost: 20% compared to design 3 [9] design 4 [9] design [14] design [15] design [12] design [19] and design [18] , 33% compared to design [19].

-Hardware complexity:

\*Number of CNOT gates: 75% compared to design 2 [13], design 3 [9] design [14], design [15], design [12], design [18] 80% compared to design 1 [13] 50% compared to design 4 [9].

\*Number of AND gates: 62,5% compared to design 3 [9], design [14], design [15], design [12],design [18] 25% compared to design 1 [13], design 2 [13],design 4 [9].

\*Number of NOT gates: 75% compared to design 1 [13], design 2 [13], 50% compared to design 3 [9], design [14], design [15], design [12], design [18].

## VI. CONCLUSION

Reversible logic occupies a important role in minimizing energy loss at the end of unused bits in the circuit compared to conventional logic computation. Our designs were able to minimize all performance criteria Number of gates CG, Number of constant inputs NCI, Quantum Cost QC, Hardware Complexity HC and especially the number of garbage outputs NGO in our design 2 to 4, 3 to 8, and  $n$  to  $2^n$ , as a result a decrease in the energy dissipated at the end of unused bits because heat is directly related to fewer garbage outputs. While waiting for new reversible gates to exploit in the future, we can optimize decoder 2 to 4, 3 to 8, and  $n$  to  $2^n$  respecting the performance, typically concerning minimizing heat energy.

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TABLE III. COMPARATIVE TABLE OF THE PERFORMANCE CRITERIA OF RECENT STUDIES OF THE N TO  $2^n$  DECODER

nto $2^n$	CG	NGO	NCI	QC	HC
OD	$2^{n-3}$	n-2	$2^{n-2}$	$4(2^{n-2})$	$(2^{n-1}+5)\alpha + (32^{n-1})+2\beta+(2^{n-1}+2)\delta$
Design1[13]	$2^{n-1}-1$	$2^{n-1}+n-4$	$32^{n-1}-4$	—	$(52^{n-1}-5)\alpha + (42^{n-1}-4)\beta+(42^{n-1}-6)\delta$
Design2 [13]	$2^{n-3}$	n-2	$2^{n-2}$	—	$(2^{n+1}-3)\alpha + (2^{n+1}-4)\beta+(2^{n+1}-6)\delta$
Design3[9]	$2^{n-1}$	n-1	$2^{n-1}$	$52^n-9$	$(2^n+1-3)\alpha + (2^{n+2}-8)\beta+(2^n-2)\delta$
Design4[9]	$2^{n-3}$	n-2	$2^{n-2}$	$52^n-13$	$(2^n+7)\alpha + (2^{n+1}+9)\beta+(2^{n-1}-3)\delta$
[14]	$2^{n-1}$	n	$2^n$	$52^n-5$	$(2^{n+1}-2)\alpha + (2^{n+2}-4)\beta+(2^n-1)\delta$
[10]	$2^{n-3}$	n	$2^n$	$52^n-9$	$(2^{n+1}-2)\alpha + (2^{n+2}-12)\beta+(2^n-3)\delta$
[12]	$2^{n-1}$	n-1	$2^{n-1}$	$52^n-11$	$(2^{n+1}-3)\alpha + (2^{n+2}-8)\beta+(2^n)\delta$
[19]	10	n	$2^n$	$62^n$	—
[18]	$2^{n-1}$	n	$2^n$	$(52^n-8)$	$(2^{n+1}-2)\alpha + (2^{n+2}-8)\beta+(2^n-2)\delta$
%Design1[13]		$(2^{n-1}-2)/(2^{n-1}+n-4)$	$(2^{n-1}-2)/(32^{n-1}-4)$		$(42^{n-1}-10)/(52^{n-1}-5) - (2^{n-1}-6)/(42^{n-1}-4) - (32^{n-1}-8)/(42^{n-1}-6)$
%Design2[13]	—	—	—		$(32^{n-1}-8)/(2^{n+1}-3) - (2^{n-1}-6)/(2^{n+1}-4) - (32^{n-1}-8)/(2^{n+1}-6)$
%Design3[9]	$2/(2^{n-1})$	$1/(n-1)$	$1/(2^{n-1})$	$(2^{n-1})/(52^{n-9})$	$(32^{n-1}-8)/(2^{n+1}-3) - (52^{n-1}-10)/(2^{n+2}-8) - (2^{n-1})/(2^{n-6})$
%Design4[9]	—	—	—	$(2^{n-5})/(52^{n-13})$	$(2^{n-1}+2)/(2^{n+7}) - (2^{n-1}-11)/(2^{n+1}-9) - (1/(2^{n-1}-3)$
%[14]	$2/(2^{n-1})$	$2/n$	$1/(2^{n-1})$	$(2^{n+3})/(52^{n-5})$	$(32^{n-1}-7)/(2^{n+1}-2) - (52^{n-1}-6)/(2^{n+2}-4) - (2^{n-1}-3)/(2^{n-1})$
%[10]		$2/n$	$1/2^{n-1}$	$(2^{n-1})/(52^{n-9})$	$(32^{n-1}-7)/(2^{n+1}-2) - (52^{n-1}-14)/(2^{n+2}-12) - (2^{n-1}-5)/(2^{n-3})$
%[12]	$2/(2^{n-1})$	$1/(n-1)$	$1/(2^{n-1})$	$(2^{n-3})/(52^{n-11})$	$(32^{n-1}-8)/(2^{n+1}-3) - (52^{n-1}-10)/(2^{n+2}-8) - (2^{n-1}-2)/(2^n)$
%[19]		$2/n$	$1/(2^{n-1})$	$(2^{n+1}+8)/(62^n)$	
%[18]	$2/(2^{n-1})$	$2/n$	$1/(2^{n-1})$	$(2^n)/(52^n-8)$	$(32^{n-1}-7)/(2^{n+1}-2) - (52^{n-1}-10)/(2^{n+2}-8) - (2^{n-1}-4)/(2^{n-2})$

TABLE IV. COMPARATIVE TABLE OF THE PERFORMANCE CRITERIA OF RECENT STUDIES OF THE N TO  $2^n$  DECODER WHEN N TENDS TO INFINITY

Decoder n à $2^n$	CG	NGO	NCI	QC	HC
% Imp Design1[13]		100	33		80 CNOT, 25 AND , 75NOT
%Imp Design2[13]					75 CNOT, 25 AND , 75NOT
% Imp Design3[9]	0	0	0	20	75 CNOT, 62,5 AND , 50NOT
% Imp Design4[9]				20	50 CNOT, 25 AND
% Imp [14]	0	0	0	20	75 CNOT, 62,5 AND , 50NOT
% Imp [15]		0	0	20	75 CNOT, 62,5 AND , 50NOT
% Imp [12]	0	0	0	20	75 CNOT, 62,5 AND , 50NOT
% Imp [19]		0	0	33	
%Imp [18]	0	0	0	20	75 CNOT, 62,5 AND , 50NOT

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