

# Energy-Efficient, Noise-Tolerant CMOS Domino VLSI Circuits in VDSM Technology

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**Abstract**— Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in dynamic logic such as domino is often used in performance critical paths, to achieve high speeds where static CMOS fails to meet performance objectives. However, domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates. Keeping in view of the above stated problems in previous existing designs, novel energy-efficient domino circuit techniques are proposed. The proposed circuit techniques reduced the dynamic switching power consumption; short-circuit current overhead, idle mode leakage power consumption and enhanced evaluation speed and noise immunity in domino logic circuits. Also regarding performance, these techniques minimize the power-delay product (PDP) as compared to the standard full-swing circuits in deep sub micron CMOS technology.

Also the noise immunity of the CMOS Domino circuits with various techniques and keepers are analyzed. Various noise sources are considered and noise immune domino logic is proposed.

**Keywords**- *Dynamic; Domino; Noise Margin; Very Deep submicron technology; High speed; Power consumption; Power delay product (PDP).*

## I. INTRODUCTION

Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. However, domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS logic circuits. In this paper novel energy-efficient domino circuit techniques are proposed.

This paper is organized as follows. In section II, Dual-rail domino circuit with self-timed precharge scheme is proposed.

The pseudo-footless dynamic circuit technique is presented in section III. Section IV describes performance evaluation results of energy-efficient dual-V<sub>t</sub> domino logic. Section V describes the Noise immune domino logic. Then conclusions are presented in section VI.

## II. DUAL-RAIL DOMINO FOOTLESS CIRCUIT WITH SELF-TIMED PRECHARGE SCHEME (DRDFSTP):

*Conventional domino circuits:*

In this section, several conventional domino circuits with their own clocking schemes are briefly reviewed.

### A. Dynamic DCVSL Footed Circuit (DDCVSLF):

Fig.1 shows AND/NAND dynamic DCVSL Footed circuit. One of the disadvantages of this kind of domino circuit is that the existence foot transistor slows the gates somewhat, as it presents an extra series resistance. Moreover, simultaneous precharge may cause an unacceptable IR-drop noise.

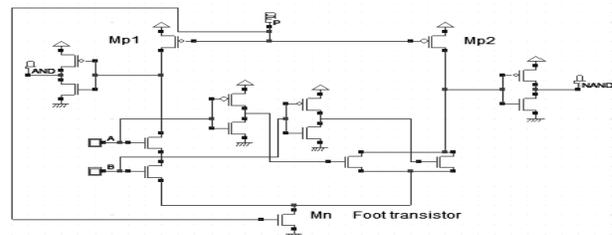


Fig.1. Dynamic DCVSL AND/NAND Footed gate

### B. Dynamic DCVSL Footless Circuit (DDCVSLFL):

Fig.2 shows AND/NAND dynamic DCVSL Footless circuit. Two benefits come from the usage of footless domino gates: improved pull-down speed and reduced precharge signal load. Main disadvantage is simultaneous precharge will cause short-circuit current.

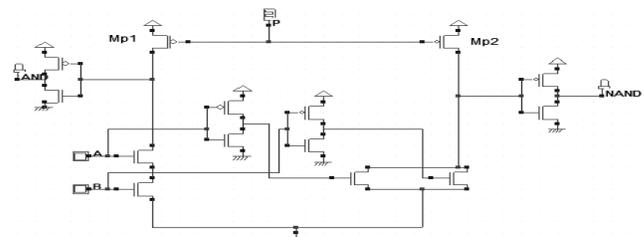


Fig. 2. Dynamic DCVSL AND/NAND Footless gate

C. Delayed-Reset Domino Circuit (DRDC):

Fig.3 illustrates the delayed-reset domino AND/NAND circuit [3]. However, the use of delay elements, together with the need of both footed and footless cell libraries tends to increase design complexity.

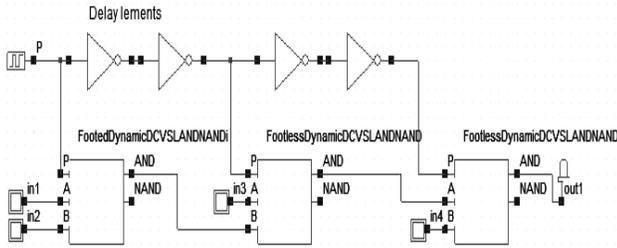


Fig.3. The delayed-reset domino AND/NAND circuit

D. Dual-Rail Data-Driven Dynamic Logic ( $D^4L$ ):

$D^4L$  circuit uses input signals instead of precharge signal for correct precharge and evaluation sequencing [5]. Correspondingly, clock-buffering and clock-distribution problems can be eliminated. Furthermore, the foot transistor can be eliminated without causing a short-circuit problem. A  $D^4L$  two-input AND/NAND gate is shown in Fig.4.

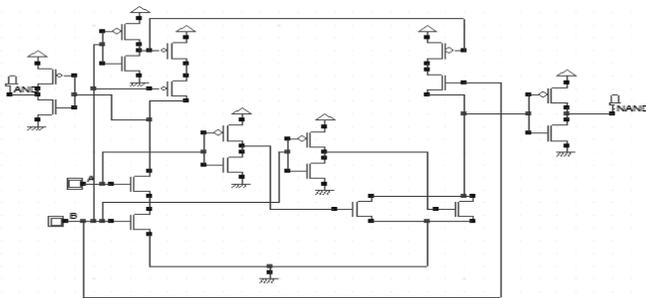


Fig.4. Dual-Rail Data-Driven Dynamic AND/NAND Logic ( $D^4L$ )

Dual-Rail Domino Footless Circuit with Self-Timed Precharge Scheme (DRDFSTP):

The presence of the foot transistor in the conventional dynamic DCVSL circuit shows the gate somewhat, as it presents an extra series resistance. To safely remove the transistor, two constraints must be met: (1) gate changes to evaluation phase before valid input come; (2) gate changes to precharge phase only after inputs change to zero. We propose a footless dual-rail domino circuit with self-timed precharge scheme to realize a high performance footless domino circuit while meeting the constraints mentioned above. It is expected that the peak of precharge current could be reduced due to the self-timed precharge scheme. Fig. 9 shows the AND/NAND gate of the proposed footless dual-rail domino circuit with self-timed precharge scheme. The self-timed precharge control logic consists of static CMOS inverter whose source of NMOS transistors are tied to input signals, which generate sub-precharge signals (PC1-PC4) from precharge signal P in cases of the corresponding input signals are zero. The PMOS precharge tree above the pull down network (PDN) is used for precharging the corresponding gate.

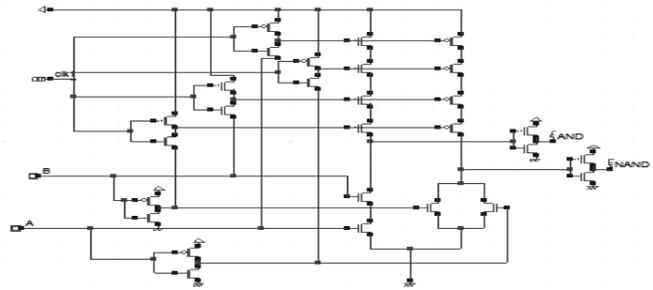


Fig:5. Dual-rail footless domino AND/NAND gate with self-timed precharge scheme.

Simulation results:

In this work, we have implemented a Dynamic DCVSL circuit, Dual-Rail Data-Driven Dynamic Logic and a proposed circuit Dual-Rail Domino Footless Circuit with Self-Timed Precharge Scheme. The results of simulation are shown in the below TABLES1-3.

Table1. AND/NAND GATE

Technique	Power ( $\mu w$ )	CriticalID elay (ns)	PDP ( $10^{-15}$ w-s)	Area ( $\mu.sqm$ )
DDCVSLF	7.6	0.088	0.6688	69.62
DDCVSLFL	152	0.025	3.8	65.41
DRDC	205	0.137	28.085	252.9
$D^4L$	72.555	0.111	8.053606	93.3
DRDFSTP	7.676	0.042	0.322392	177.6

Table2. OR/NOR GATE

Technique	Power ( $\mu w$ )	CriticalID elay (ns)	PDP ( $10^{-15}$ w-s)	Area ( $\mu.sqm$ )
DDCVSLF	7.58	0.087	0.65946	74.82
DDCVSLFL	145	0.090	13.05	66.59
DRDC	220	0.403	88.66	290
$D^4L$	10.163	0.112	1.138256	78.48
DRDFSTP	7.583	0.042	0.318486	30.18

Table3. XOR/XNOR GATE

Technique	Power ( $\mu w$ )	Critical Delay (ns)	PDP ( $10^{-15}$ w-s)	Area ( $\mu.sqm$ )
DDCVSLF	11.7	0.032	0.3744	99.2
DDCVSLFL	99.023	0.032	3.1687	92.17
DRDC	231	0.091	21.021	391.9
$D^4L$	16.802	0.029	0.487258	100.5
DRDFSTP	11.642	0.04	0.46568	200.13

III. PSEUDO FOOTLESS DOMINO CIRCUIT (PF-DOMINO)

Footed domino circuit with a global clock:(FD)

Fig. 6 shows the most conventional domino circuit, which comprises of footed domino gates driven by a common clock

buffer. One of the disadvantages of this kind of domino circuit is that it should be constructed with only true-logic gates. Moreover, simultaneous precharge may cause an unacceptable IR-drop noise.

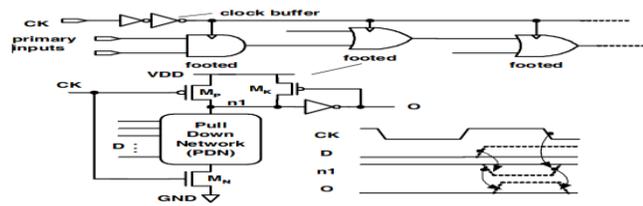


Fig. 1 The footed domino gate

Fig.6. The footed domino gate

*Footless domino circuit with delayed clocks:(DR-domino)*

Fig.7 illustrates the delayed-reset domino circuit (DR-domino). The DR-domino circuit does not improve the logic construction flexibility because it still accepts true logic gates only.

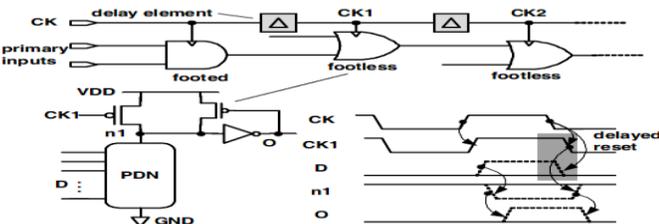


Fig. 2 The DR-domino circuit

Fig.7. The DR-domino circuit

*Footed domino circuit with delayed clocks:*

In order to improve the logic construction flexibility, the Clock-Delayed domino (CD-domino) circuit, shown in Fig. 8, is proposed to allow the usage of both positive and negative logic gates within a block. To achieve this flexibility, the clock rising edge of a gate should be delayed until all the incoming data settle. However, the delayed evaluation and the footed gates degrade the performance of the whole circuit seriously.

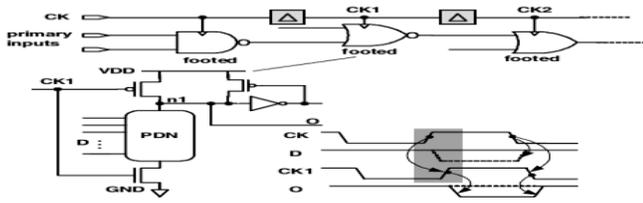


Fig. 3 The CD-domino circuit

Fig. 8. The CD-domino circuit

In this work, we start from adopting an improved delayed-evaluation clocking style to preserve the logic construction flexibility, but add new circuit techniques to remove the other origin of speed limitation, i.e. the usage of footed gates.

*Pseudo footless domino circuit :( PF-domino):*

The pseudo footless domino circuit (PF-domino) is shown in Fig. 9. Basically, the circuit structure of the PF-domino is exactly the same with that of the CD-domino circuit. The differences lie in two aspects. First, all the logic gates used are pseudo-footless (PF) dynamic gates (as the inserted gate

shows), rather than footed gates. Second, an enhanced self-timed delayed-evaluation clocking scheme is used to replace the simple clock-delayed scheme used in the CD-domino circuit. These two techniques are introduced in the following step by step.

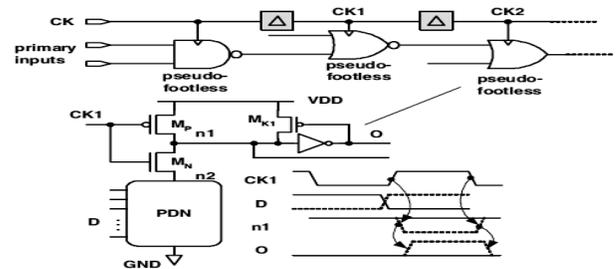


Fig. 4 The PF-domino circuit with the primitive PF gate

Fig.9. The PF-domino circuit with primitive PF gate

*The pseudo-footless dynamic gates:*

The pseudo-footless dynamic circuit technique was first proposed. The PF gate inserted in Fig. 9 is the primitive version used, which is quite similar to a typical footed domino gate except that  $M_N$  is pulled up beneath  $M_P$ . The preferred PDN function is NOR. Such an arrangement is beneficial for both speed and power. First, for the dynamic part, only a small output node is precharged, and then the discharged charge, if necessary, is much smaller than that of a conventional footed gate. Second, we require that all the data inputs be ready before the clock rises up. Then, before the evaluation phase, most charges in the PDN have been discharged, which results in a very high-speed discharge in the evaluation phase. This mechanism is also the name “pseudo-footless” comes from.

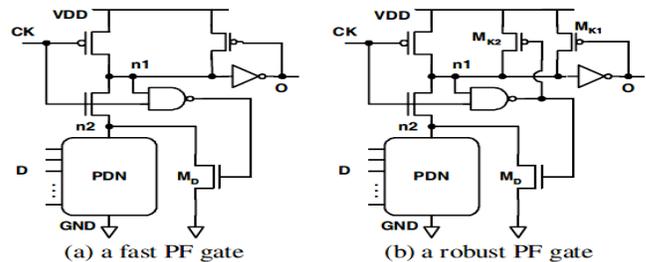


Fig. 5 Derivatives of the primitive PF gate

Fig.10. Derivatives of the primitive PF gate

When used in a general domino environment, the PDN may realize a complicated large-fan-in function. The increased capacitance at node  $n2$  will slow down the discharge. The circuit shown in Fig. 10(a) is proposed for speeding in such a condition. The transistor  $M_D$  is added in parallel with the PDN and is activated in the precharge phase to deplete the charge at  $n2$  in advance. During evaluation,  $M_D$  is initially disabled because  $n1$  is high. If  $n1$  is being pulled down,  $M_D$  will be turned on to help discharge. This gate is called a fast PF gate. When the capacitance of  $n2$  is much larger than that of  $n1$ , we need to consider the problem of charge sharing. In this case, we can use the gate shown in Fig. 10(b), a robust PF gate, where a second keeper  $M_{K2}$  is added to replenish the charge to  $n1$  when it is subject to a voltage fluctuation due to a charge sharing condition. The output loading and the fan-in number are the dominant factors that determine the performance of PF gates.

Hence, we need to find out which type of the PF gate is the best choice for each loading and fan-in combination. First, different PF gates with different fan-in numbers are designed and characterized for various loading conditions. And second, the fastest circuit without the charge sharing effect is considered to be the best choice.

*The enhanced self-timed delayed-evaluation:*

The delay element is the key component for the speed, as explained in the following. If a gate receives all non-inverted inputs, the arrival time of the clock rising edge will not cause malfunction. In this case, the clock signal is usually designed to arrive ahead of the data inputs so that a higher speed can be obtained. For a gate with at least one pull-down path controlled by inverted inputs, the clock signal should be delayed until all the data inputs settle to avoid an unrecoverable error. An enough margin of this delay must be kept to face the PVT variations. In the CD-domino circuit, a simple buffer-type delay element is mentioned, which asks for a quite large margin of the delay and causes remarkable performance degradation. We propose to use a more robust self-tracking.

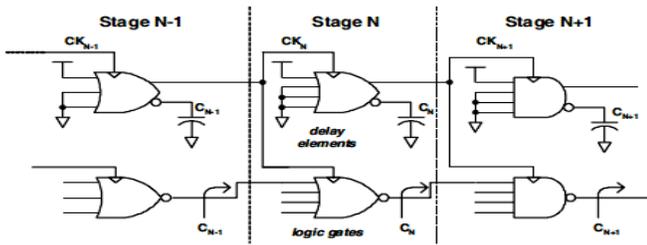


Fig. 6 The proposed robust self-tracking scheme

Fig. 11. The proposed robust self-tracking scheme

*Simulation results:*

Using the above techniques OR2 gate, AND2 gate, XOR2 gate are implemented. These design styles are compared by performing detailed transistor-level simulations on benchmark circuits using DSCH3 and Microwind3 CAD tool for 65 nm technology.

Table4.AND2 Gate

Technique	Power( $\mu$ w)	Delay(ns)	PDP(*10-15)	Area(s q. $\mu$ m)	Noise Immunity(mv)
FD	10.045	0.045	0.452025	29.64	10
DLRF LD	201.00	0.045	9.045	94.82	40
DLRF D	10.047	0.045	0.452115	28.54	30
PSFLD	10.006	0.050	0.5003	26.31	30
Fast PSFLD	160.00	0.064	10.24	58.08	40
Robust PSFLD	159.00	0.100	15.9	57.51	60

Table5.OR2 Gate

Technique	Power( $\mu$ w)	Delay(ns)	PDP(*10-15)	Area(s q. $\mu$ m)	Noise Immunity(mv)
FD	5.7760	0.044	0.254144	31.92	50
DLRF LD	94.589	0.044	4.161916	21.43	70
DLRF D	5.7660	0.044	0.253704	28.54	100
PSFLD	5.5600	0.047	0.261320	25.94	100
Fast PSFLD	110.00	0.066	7.260000	47.35	120
Robust PSFLD	111.00	0.102	11.32200	53.51	120

Table6. XOR2 Gate

Technique	Power( $\mu$ w)	Delay(ns)	PDP(*10-15)	Area(s q. $\mu$ m)	Noise Immunity(mv)
FD	33.709	0.082	2.764138	83.26	10
DLRF LD	63.697	0.049	3.121153	62.97	10
DLRF D	18.078	0.049	0.885822	56.17	10
PSFLD	1.4290	0.052	74.308	53.84	10
Fast PSFLD	166.00	0.066	10.956	83.42	10
Robust PSFLD	167.00	0.073	12.191	89.43	90

IV. ENERGY-EFFICIENT DUAL- $V_T$  DOMINO LOGIC

A. Standard single threshold ( low- $V_t$  ) voltage

In this, all standard low-threshold voltage transistors (  $V_t = 0.4$  volts ) are used in implementing the bench mark circuits and are simulated using DSCH and Microwind 3.1.

B. Standard single threshold ( high- $V_t$  ) voltage

In this, all standard high-threshold voltage transistors (  $V_t = 0.7$  volts ) are used in implementing the bench mark circuits .

C. Standard dual threshold voltage

This Dual Threshold CMOS (DTCMOS) design technique uses fast low threshold voltage (LTV) and slow high threshold voltage (HTV) devices. Thus, the aim of DTCMOS is to maximize the gain in leakage at the HTV devices without worsening the performance of the circuit. In this, the PMOS and NMOS transistors in the output inverter are used with high  $V_t$  and remaining are used with low  $V_t$  devices.

D. Modified dual- $V_t$  technology

This technology is the proposed technology, which is a modification of standard dual-threshold technology. In standard dual- $V_t$  technology, the transistors of the output inverter circuit in CMOS domino logic are introduced with high- $V_t$  transistors. In this modified dual- $V_t$  technology, only the pull-down transistor is introduced with the standard high- $V_t$  transistor and

the pull-up transistor is introduced with standard low- $V_t$  transistor.

**Simulation results:**

In this work, we implemented benchmark circuits using the above four technologies. The figure of merit used to compare these technologies is Power-Delay Product (PDP). The benchmark circuits implemented in this work are and2, or2, or8, or16, xor2, 16-bit adder, 16-bit comparator, D-Latch, 4-bit LFSR which are given below from Table1-9. The OR2 gate is illustrated for the proposed technologies which are given below in Figures 12,13, 14, 15 .

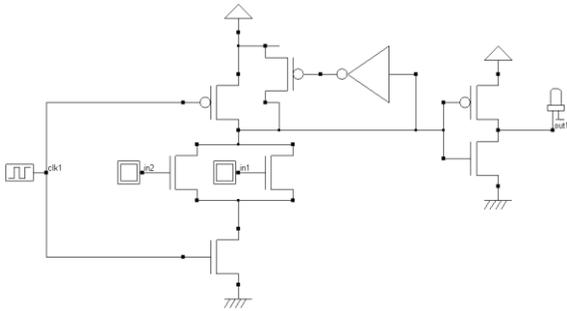


Fig.12. OR2 Standard Low- $V_t$

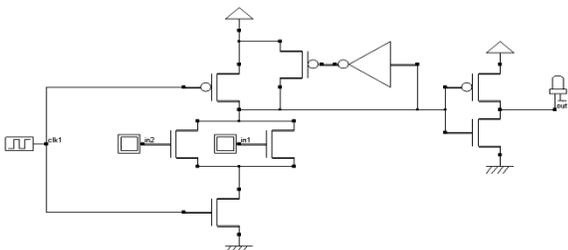


Fig.13. OR2 Standard High- $V_t$

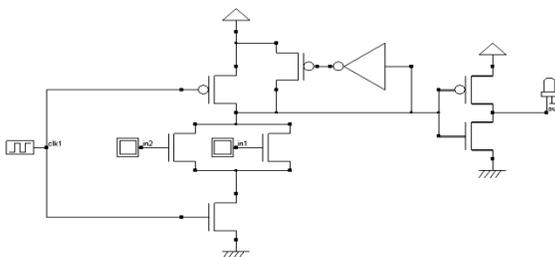


Fig.14. OR2 Standard Dual- $V_t$

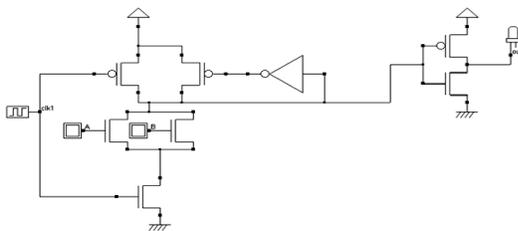


Fig.15. OR2 Modified Dual- $V_t$

Table7.16 Bit Adder

Technique	Power(mw)	Delay(ns)	PDP (10 <sup>-12</sup> w-s)	Area (μ.sqm)
Standard low $V_t$	6.359	55.416	352.39	10841.32
Standard high $V_t$	6.270	54.943	344.49	12518.60
Standard Dual $V_t$	6.262	56.219	352.04	11294.89
Modified Dual $V_t$	6.270	60.967	382.26	12950.92

Table8.16 Bit Comparator

Technique	Power(mw)	Delay(ns)	PDP (10 <sup>-12</sup> w-s)	Area (μ.sqm)
Standard low $V_t$	6.648	74.557	495.654	18294.44
Standard high $V_t$	6.619	71.155	470.974	19835.87
Standard Dual $V_t$	6.637	67.751	449.663	18505.20
Modified Dual $V_t$	6.634	80.915	536.790	19306.26

Table9.D Latch

Technique	Power(mw)	Delay(ns)	PDP (10 <sup>-12</sup> w-s)	Area (μ.sqm)
Standard low $V_t$	0.189	0.307	0.058	259.86
Standard high $V_t$	0.221	0.389	0.085	273.16
Standard Dual $V_t$	0.223	0.429	0.095	291.04
Modified Dual $V_t$	0.221	0.352	0.077	259.86

Table10.4 Bit LFSR

Technique	Power(mw)	Delay(ns)	PDP (10 <sup>-12</sup> w-s)	Area (μ.sqm)
Standard low $V_t$	3.748	3.192	11.963	2682.39
Standard high $V_t$	4.037	3.583	14.464	2861.61
Standard Dual $V_t$	4.033	3.735	15.063	2733.37
Modified Dual $V_t$	4.008	3.532	14.156	2795.82

Table11. OR8 gate

Technique	Power(μw)	Delay(ns)	PDP (10 <sup>-15</sup> w-s)	Area (μ.sqm)
Standard low V <sub>t</sub>	0.892	0.088	0.078	80.25
Standard high V <sub>t</sub>	0.990	0.143	0.141	82.16
Standard Dual V <sub>t</sub>	0.789	0.130	0.102	81.06
Modified Dual V <sub>t</sub>	0.845	0.095	0.080	81.46

Table12. OR2 gate

Technique	Power(μw)	Delay(ns)	PDP (10 <sup>-15</sup> w-s)	Area (μ.sqm)
Standard low V <sub>t</sub>	1.443	0.064	0.092	32.16
Standard high V <sub>t</sub>	1.726	0.119	0.205	32.41
Standard Dual V <sub>t</sub>	1.212	0.106	0.128	32.96
Modified Dual V <sub>t</sub>	1.355	0.071	0.096	32.23

V. NOISE IMMUNE DOMINO LOGIC CIRCUITS

In DOMINO gates, noise immunity is sacrificed for high performance. The DC noise margin of DOMINO gates is equal to the threshold voltage of pull-down transistors. Unlike static CMOS gates, the charge lost from dynamic node due to noise cannot be restored in DOMINO gates. This makes DOMINO gates more vulnerable to noise than static CMOS gates. A keeper is used to restore any loss of charge from the dynamic node. An analytical noise model for DOMINO gates where the effect of keeper is taken into account is considered.

Noise Margin:

The maximum voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case input level without causing the output voltage to deviate from the allowable logic voltage level.

A typical n-type domino CMOS logic gate as shown in Fig. 9, consists of clock controlled transistor M1 and M2, a pull-down n-type transistor network, and an output driver. The operation of a domino CMOS logic gate can be divided into two phases. In the pre charge phase when the clock CLK is low, the dynamic node is charged to logic high through

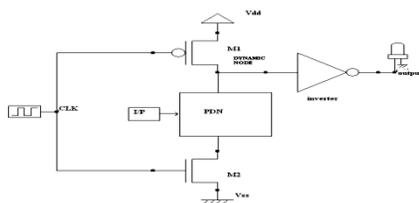


Fig. 16 domino logic

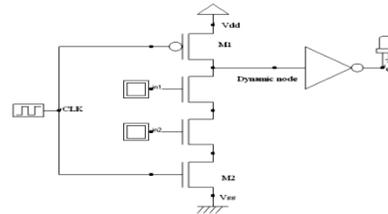


Fig.17. two input and gate

M1 and the output of the not gate is low. The evaluation phase starts when the clock goes high. In this phase, M1 is OFF and M2 is ON. The dynamic node discharges or retains its charge depending on the inputs to the pull-down network. A two input AND gate is illustrated in Fig.17.

Noise sources in dynamic logic circuits can be broadly classified into two basic types:

- 1) Gate internal noises, including charge sharing noise, leakage noise etc.,
- 2) External noises, including input noise, power and ground noise, and substrate noise.

Domino Noise Model:

Fig.18 describes the noise model for DOMINO gates.

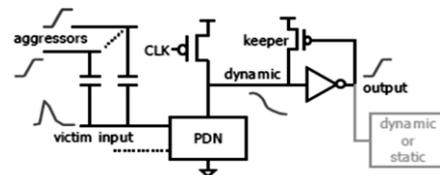


Fig.18. Crosstalk noise model for domino gates

Domino Noise Margin:

In order to obtain an analytical solution for noise margin for DOMINO gates, consider the current model for the PDN NMOS transistor.

We define the DOMINO noise margin as

$$DNM_{DOMINO} = \frac{NM_{inv} \cdot C_d + \left[ \frac{1}{2} \cdot T \cdot I_{k\_Max} \right]}{g_m}$$

Note that the keeper effect does not contribute to any extra computational cost since T is obtained from the already available input noise pulse and I<sub>k-max</sub> can also be pre-characterized.

Circuit Techniques for Noise immune Domino Logic:

Internal nodes precharging: (PCIN)

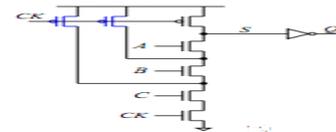


Fig.19. internal nodes Precharchig

A simple effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull-down

network along with precharging the dynamic node. An example of dynamic 3-input AND gate using this technique is illustrated in Fig.19. Finally, it is noted that techniques based on precharging internal nodes alone are not very effective against external noises.

**Pull-up Technique with PMOS: (PPTQ)**

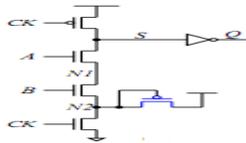


Fig.20. pull-up technique with PMOS

The pull-up technique, shown in Fig. 20, employs a PMOS transistor at node N2 forming a resistive voltage divider with the bottom clock controlled transistor. One major drawback of this technique is the DC power consumption in the resistive voltage divider. Furthermore, since the voltage level at the dynamic node S can never get lower than the voltage at node N2, the voltage swing at node S is not rail-to-rail. When the size of the PMOS pull-up transistor is large in an effort to aggressively raise gate noise immunity, the gate output may also not have a rail-to-rail swing.

**NMOS Pull-up Technique: (NPTQ)**

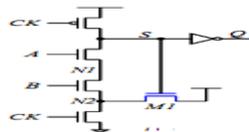


Fig.21. NMOS pull-up technique

An improved method, shown in Fig. 21, employs a pull-up transistor with feedback control. Here an NMOS transistor M1 is used to pull up the voltage of an internal node. This design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low, therefore, the dynamic node S undergoes rail-to-rail voltage swing. Also, the DC power consumption problem is partially solved.

**Feedback NMOS Mirror Technique: (MRTQ)**

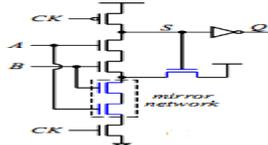


Fig.22. Feedback NMOS Mirror technique

The mirror technique employs a feedback controlled NMOS transistor similar to the NMOS pull-up technique. In addition, it duplicates the pull-down network in an effort to further reduce DC power consumption and to further improve gate noise tolerance. A 2-input dynamic AND gate designed using the mirror technique is shown in Fig. 22. However, this technique significantly lengthens the discharge path in the pull-down network, which potentially leads to slower circuit or considerably increased circuit active area when the transistors are aggressively sized.

**NMOS Two Transistor Technique: (TTTQ)**

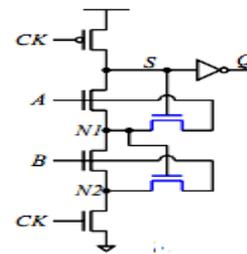


Fig.23. NMOS Two transistor technique

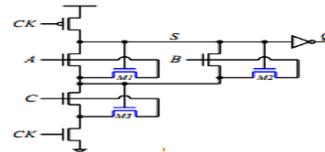


Fig.24. A 3-input OR-AND gate

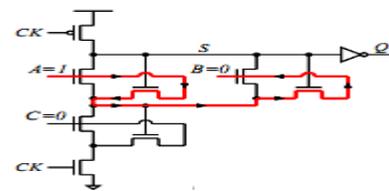


Fig.25. Direct conducting path.

The NMOS two transistor technique adopts NMOS pull-up transistors at all internal nodes to further improve dynamic gate noise immunity. In addition, the drain nodes of the pull-up NMOS transistors are connected to the inputs instead of to the power-supply network, as illustrated in Fig.23. As an example, in Fig.24, we show a 3-input OR-AND gate implementing the logic function of  $(A + B).C$ . Assume input A is high while inputs B and C are low. The dynamic node S stays high because C is low and there is no discharging path to the ground. Under such scenario, there is a DC conducting path between the two inputs A and B, as illustrated in Fig.25.

**Complementary weak P-Network Technique: (CPNTQ)**

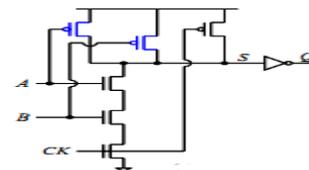


Fig.26. Complementary weak p-network technique

The basic principle of this class of techniques is to construct a weak complementary p-network to prevent the dynamic node from being floating in the evaluation phase. One such technique is illustrated in Fig. 26. In addition to the silicon area overhead associated with the pull-up network, a major drawback of this technique in practice is its ineffectiveness in dealing with very wide logic gates, for example, wide OR gates, where dynamic logic styles really outshine static CMOS logic gate in performance.

**Inverter Technique: (CMITQ)**

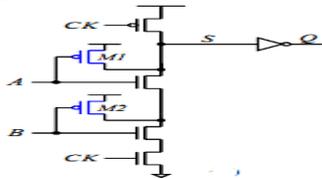


Fig.27(a). inverter circuit

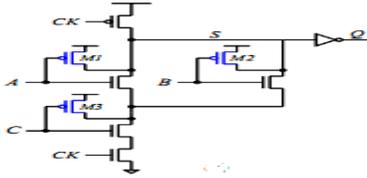


Fig.27(b) A 3- input OR-AND gate.

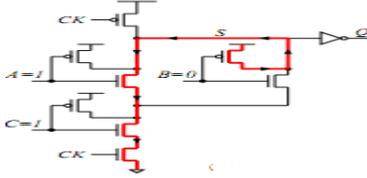


Fig.27(c) Direct conducting path

PMOS transistors can also be employed at a per transistor level, as shown in Fig. 27. This technique is known as inverter technique.

**Inverter Gated Technique: (GCMITQ)**

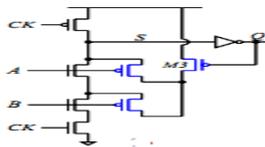


Fig: 28. inverter gated technique

In Fig: 27(a), for example, if input A stays high and input B falls from high to low during the evaluation phase, the dynamic node may be reset to high by the pull-up PMOS transistor M2. With a view to solve this false reset problem, an additional transistor M3 is used shown in Fig. 28, it is called inverter gated technique.

**Three Transistor Technique: (TTRTQ)**

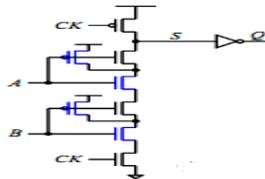


Fig.29. Three transistor technique

Figure 29 illustrates a noise-tolerant 2-input AND gate using a triple transistor technique, where each NMOS transistor in the pull-down network of a simple dynamic logic gate is replaced by three transistors.

**Noise immune logic using different keepers:**

**Domino Always on Keeper (DAOK):**

Always On Keeper uses ‘weak’-PMOS device between the output node and  $V_{DD}$  as shown in Figure 30. As the gate is

connected to GND, this PMOS device will always be turned ON. So, even in the evaluation phase, the output node will be connected in some capacity to  $V_{DD}$ . The PMOS ‘keeper,’ has the effect of maintaining the output node charge even at slower clock speeds.

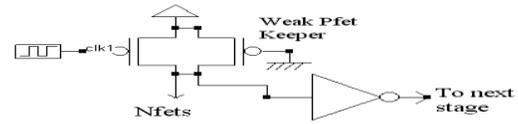


Fig.30. Domino always on keeper

Although this configuration has advantages, it does introduce another PMOS device into each stage and also causes excess power dissipation due to possibility of the connection from  $V_{DD}$  to GND through the NMOS devices and the PMOS keeper.

**Domino Feedback Keeper (DFBK):**

The use of a keeper PMOS in dynamic logic could be further improved by connecting the gate of the keeper not to GND, but to the output node of the inverter stage as shown in Figure 31.

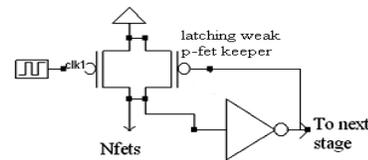


Fig: 31.Domino Feedback keeper

The keeper would now function as a latch cutting off whenever the output of the inverter is high. In this way, power dissipation is significantly reduced whenever a pull-down path to GND has been formed in the NMOS logic block since this would make the input to the inverter low and thus the output of the inverter high. When the output of the inverter is low however, as would be the case if no pull-down path to ground was formed in the NMOS logic block, the keeper PMOS would turn on and maintain the output high charge on the precharge node even at reduced clock speeds or an idle.

**Domino Standard Keeper (DSTDK):**

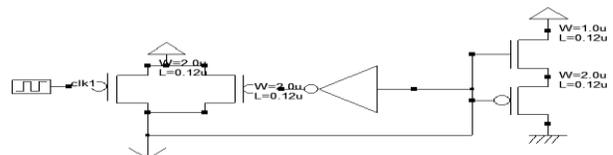
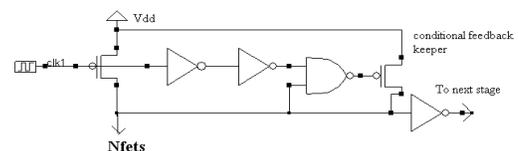


Fig.32. Standard keeper

**Domino Modified Feedback Keeper (DMDFBK):**





OR2 (65nm Technology):

Table16. OR2 gate

S.NO	CIRCUIT TECH	PROPAGATION DELAY(nsec)	POWER DISSIPATION (μW)	PDP (x10 <sup>-18</sup> )	NOISE MARGIN(m V) [POWER (μw)]	AREA (μ- mts <sup>2</sup> )	NO.OF SYMBOLS
1	DAOK	0.025	0.172	4.3	250[67.497]	21.17	13
2	DFBK	0.050	0.173	8.65	220[54.589]	21.36	12
3	DSTDK	0.064	7.264	464	220[67.237]	30.17	16
4	DMDFBK	0.034	0.551	18	740[167]	31.89	15
5	DMDFBKHP	0.036	0.539	19	950[182]	35.19	16

OR4 (65nm Technology):

Table17. OR4 gate

S.NO	CIRCUIT TECH	PROPAGATION DELAY(nsec)	POWER DISSIPATION (μW)	PDP (x10 <sup>-18</sup> )	NOISE MARGIN(m V) [POWER (μw)]	AREA (μ- mts <sup>2</sup> )	NO.OF SYMBOLS
1	DAOK	0.033	76.042	2500	100[74.599]	34.27	17
2	DFBK	0.062	0.733	45	220[27.158]	34.27	16
3	DSTDK	0.072	1.019	73	330[50.026]	45.50	20
4	DMDFBK	0.047	0.742	34	1500[210]	47.29	19
5	DMDFBKHP	0.044	0.743	32	1700[220]	80.63	28

XOR2 (65nm Technology):

Table18. XOR2 gate

S.NO	CIRCUIT TECH	PROPAGATION DELAY(nsec)	POWER DISSIPATION (μW)	PDP (x10 <sup>-18</sup> )	NOISE MARGIN(m V) [POWER (μw)]	AREA (μ- mts <sup>2</sup> )	NO.OF SYMBOLS
1	DAOK	0.034	21.788	740	120[6.323]	42.08	17
2	DFBK	0.048	21.791	1045	140[17.187]	42.08	16
3	DSTDK	0.069	22.206	1532	140[18.81]	50.71	20
4	DMDFBK	0.051	1.755	89	380[6.360]	53.07	19
5	DMDFBKHP	0.048	19.507	936	400[17.402]	56.59	20

8-Bit MUX(65nm Technology):

Table19. 8-Bit MUX

S.NO	CIRCUIT TECH	PROPAGATION DELAY(nsec)	POWER DISSIPATION (μW)	PDP (x10 <sup>-18</sup> )	NOISE MARGIN(m V) [POWER (μw)]	AREA (μ- mts <sup>2</sup> )	NO.OF SYMBOLS
1	DAOK	0.058	53.854	3123	230[138]	135.58	40
2	DFBK	0.063	53.92	3396	230[138]	135.55	39
3	DSTDK	0.073	13.183	962	100[18.117]	151.03	43
4	DMDFBK	0.039	13.251	516	100[19.730]	149.92	42
5	DMDFBKHP	0.031	13.075	405	100[19.217]	160.82	43

16-Bit MUX(65nm Technology):

Table20. 16-Bit MUX

S.NO	CIRCUIT TECH	PROPAGATION DELAY(nsec)	POWER DISSIPATION ( $\mu$ W)	PDP ( $\times 10^{-18}$ )	NOISE MARGIN(mV) [POWER ( $\mu$ W)]	AREA ( $\mu$ -mts <sup>2</sup> )	NO.OF SYMBOLS
1	DAOK	0.090	25.463	2291	180[107]	392.3	72
2	DFBK	0.104	25.536	2655	120[38.303]	395.2	71
3	DSTDK	0.105	13.510	1418	70[18.424]	419.2	75
4	DMDFBK	0.095	13.440	1276	70[16.836]	419.8	74
5	DMDFBKHP	0.097	13.462	1305	70[17.039]	428.7	75

Table21.4 Input OR gate

S . N O	Technique	Power Dissipation( $\mu$ w)	Prop agation Dela y(ns)	PDP (10 <sup>-18</sup> w-s)	Nois e Mar gin(mv) [po wer( $\mu$ w)]	Ar ea ( $\mu$ . sq m)	N o of Sy m bo ls
1	PC IN	0.810	0.024	19.44	60[1.83]	32.19	15
2	PP TQ	204	0.028	5712	270[260]	38.67	17
3	NP TQ	53.74	0.028	1504	200[60.71]	40.29	17
4	M RT Q	2.129	0.045	958.05	250[37.55]	63.14	21
5	TT TQ	39.52	0.097	3833	50[40.08]	55.35	19
6	CP NT Q	34.47	0.086	2964	220[71.50]	98.43	19
7	C MI TQ	34.57	0.192	6638	210[67.97]	93.03	23
8	GC MI TQ	2.546	0.039	99.29	430[73.24]	59.41	20
9	TT RT Q	1.922	0.031	59.58	280[75.08]	81.37	27

Table22..2 Input AND gate

S . N O	Technique	Power Dissipation( $\mu$ w)	Prop agation Dela y(ns)	PDP (10 <sup>-18</sup> w-s)	Nois e Mar gin(mv) [po wer( $\mu$ w)]	Ar ea ( $\mu$ . sq m)	N o of Sy m bo ls
1	PC	0.431	0.01	81.8	350[	26.	12

	IN		9	9	45.55]	20	
2	PP TQ	64.236	0.025	1605	300[80.81]	25.16	13
3	NP TQ	43.006	0.037	1591	470[71.49]	24.66	13
4	M RT Q	0.558	0.032	17.85	360[28.30]	34.81	15
5	TT TQ	0.391	0.034	13.29	60[4.48]	34.98	13
6	CP NT Q	0.397	0.045	17.86	260[25.81]	29.62	13
7	C MI TQ	13.764	0.043	591.85	160[22.19]	30.64	15
8	GC MI TQ	0.485	0.030	14.55	340[38.29]	35.23	14
9	TT RT Q	0.780	0.031	24.18	150[21.67]	23.34	17

## VI. CONCLUSIONS

This work consists of four parts. In section II the circuits Dynamic DCVSL footed circuit, Dynamic DCVSL footless circuit; Dual-Rail Data-Driven Dynamic Logic and Dual-rail Footless domino gate with self-timed precharge scheme are successfully implemented using CMOS domino logic. The proposed circuits have offered an improved performance in power dissipation, speed and noise tolerance when compared with standard domino circuit. In section III, Pseudo footless domino circuit is proposed. The proposed circuit offers better performance. In section IV, energy-efficient domino logic is presented. Among the four techniques, the standard dual  $V_t$  and modified dual  $V_t$  offer better performance. In section V, an attempt has been made to simulate the noise immunity of the benchmark domino circuits with different techniques and keeper transistors which are the basic building blocks for high performance. The proposed circuits have offered an improved performance in power dissipation and noise tolerance when compared with standard domino circuit. As it is observed from the results, the DMDFBK and DMDFBKHP have lower PDP, high noise immunity. Hence, it is concluded that the proposed designs will provide a platform for designing high performance and low power digital circuits and high noise immune digital circuits such as, processors and multipliers.

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