Design and Analysis of a Novel Low-Power SRAM Bit-Cell Structure at Deep-Sub-Micron CMOS Technology for Mobile Multimedia Applications

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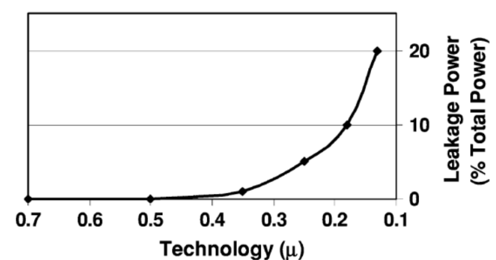
Abstract— **The growing demand for high density VLSI circuits and the exponential dependency of the leakage current on the oxide thickness is becoming a major challenge in deep-sub-micron CMOS technology. In this work, a novel Static Random Access Memory (SRAM) Cell is proposed targeting to reduce the overall power requirements, i.e., dynamic and standby power in the existing dual-bit-line architecture. The active power is reduced by reducing the supply voltage when the memory is functional and the standby power is reduced by reducing the gate and sub-threshold leakage currents when the memory is idle. This paper explored an integrated approach at the architecture and circuit level to reduce the leakage power dissipation while maintaining high performance in deep-submicron cache memories. The proposed memory bit-cell makes use of the pMOS pass transistors to lower the gate leakage currents while full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. To further reduce the leakage current, the stacking effect is used by switching off the stack transistors when the memory is ideal. In comparison to the conventional 6T SRAM bit-cell, the total leakage power is reduced by 50% while the cell is storing data '1' and 46% when data '0' at a very small area penalty. The total active power reduction is achieved by 89% when cell is storing data 0 or 1. The design simulation work was performed on the deep-sub-micron CMOS technology, the 45nm, at 25^0C with V_{DD} of 0.7V.**

Keywords- SRAM Bit-Cell; Gate Leakage; Sub-threshold Leakage; NC-SRAM; Asymmetric SRAM; PP-SRAM; Stacking Effect.

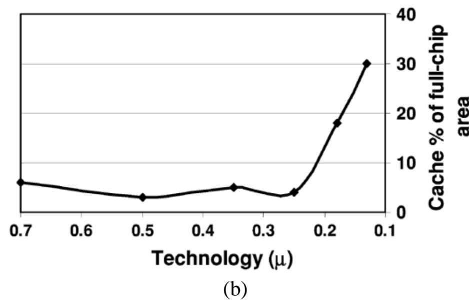
I. INTRODUCTION

Today's mobile/multimedia applications, e.g., a combination of text, audio, still images, graphics (discrete media) and audio, animation, video, video on demand, video recording, interactivity content forms (continuous media), etc. need to be incorporated in one digital system. So, there is a strong need to reduce the standby current leakage while keeping the memory cell data unchanged [1]. In other words, it demands the processor with high processing power, high performance, and low-power on-chip memory. According to the ITRS-2003 (International Technology Roadmap), 90% of the chip-area will be occupied by the memory core by 2014 [2]. This shows the more demand for chips with high functionality and low-power consumption. It is important to focus on minimizing the leakage power of the SRAM structures [3]. The main source for dynamic power consumption is through the switching. But there are several sources for the leakage current, i.e., the sub-threshold current due to low threshold voltage, the gate leakage current due to very thin gate oxides, etc., [4]. The MOS transistor miniaturization also introduces many new challenges in Very Large Scale Integrated (VLSI) circuit designs, such as sensitivity to process variations and increasing transistor leakage. In Fig.1, the leakage power from a high-performance microprocessor has been shown. It increases steadily, as the technology is scaled down [5].

A high-performance VLSI chip also demands ever increasing on-die SRAM to meet the performance needs. This pushes the SRAM scaling towards a more concern domain in today's VLSI design applications. The SRAM cell stability is further degraded by supply voltage scaling. The SRAM leakage power has also become a more significant component of total chip power as a large portion of the total chip transistors directly comes from on-die SRAM. Since the activity factor of a large on-die SRAM is relatively low. So, it is recommended by the researchers in the field to be more effective to put it in a power reduction mechanism dynamically, which modulates the power supply along the memory addressable unit or bank and the need for active/standby mode of operation. In this work, a novel technique of full-supply body-biasing scheme is devised to meet it.



(a)



(b)

Fig.1. (a) Leakage Power Percentage of Total Power. (b) Cache Area Percentage of Total Chip Area [5].

In this work we have presented a novel P4-SRAM Bit-Cell in CMOS deep-sub-micron technology that reduces the active and leakage power in the Conventional SRAM Bit-Cells. In the proposed design, contrary to "...static power is much more important than dynamic power in large memories, static power saving will very well compensate for the increase in dynamic power dissipation [3]" by giving the equal importance to the active mode of power requirements, we focus on both the dynamic and static power dissipations in the active and inactive mode of operations where the SRAM Bit-Cell is fully functional (performing write/read operations) and fully powered ON, i.e., hold state (no read/write operation). The proposed bit-cell utilizes the Gated-V_{DD} technique for transistor stacking in the PP-SRAM along with the full-supply body biasing to reduce the active, standby, and dynamic power in the memory. To the best of my knowledge, the full-supply body biasing along with pMOS stacking is being used for the first time to reduce the overall leakage in the memory cell.

The rest of the paper is organized as follows, in Section II, a basic overview of the SRAM Bit-Cell is presented. In Section III, a review of the related work is presented. In Section IV, the proposed work on a Low-leakage SRAM Bit-Cell is presented which is followed by the Simulation work and Conclusions in Sections V and VI, respectively.

II. THE CONVENTIONAL 6T-SRAM BIT-CELL

The conventional SRAM (CV-SRAM) cell has Six transistors, Fig.2. Unlike DRAM it doesn't need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of one transistor and one capacitor thereby increasing the complexity of the cell [6].

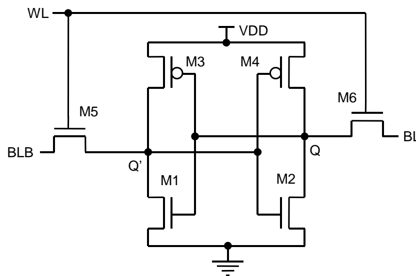


Fig. 2. A 6T-CMOS SRAM Cell [6]

The SRAM Bit Cell

The memory bit-cell has two inverters connected back to back. Two more pass transistors (M5 and M6 in Fig.1) are the access transistors controlled by the Word Line (WL). The cell preserves its one of two possible states to denote '0' and '1', as long as power is available to the bit-cell. Here, Static power dissipation is very small.

Thus the cell draws current from the power supply only during switching. But ideal mode of the memory is becoming of more concern in the deep-sub-micron technology due to is leakage power (gate, sub-threshold leakage, etc.) and data retentation at lower voltages.

The Operation of SRAM Bit-Cell

Although the two nMOS and pMOS transistors of SRAM memory bit-cell form a bi-stable latch, there are mainly the following three states of SRAM memory cell [7], the Write, Read, and Hold states.

A. Standby Operation (Hold)

When WL = '0', M5 and M6 disconnect the cell from Bit-Lines (BL and BLB). The two cross-coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are disconnected from the outside world. The current drawn in this state from the power supply is termed as standby current.

B. Data Read Operation

Read cycle starts with pre-charging BL and BLB to '1', i.e., V_{DD}. Within the memory cell M1 and M4 are ON. Asserting the word line, turns ON the M5 and M6 and the values of Q and Q' are transferred to Bit-Lines (BL and BLB). No current flows through M6, thus M4 and M6 pull BL upto V_{DD}, i.e., BL = '1' and BLB discharges through M1 and M5. This voltage difference is sensed and amplified to logic levels by sense amplifiers.

C. Data Write Operation

The value to be written is applied to the Bit lines. Thus to write data '0', we assert BL=0, BLB = '1' and to write data '1', the BL = '1', BLB = '0', asserted when WL = '1'.

III. A REVIEW OF RELATED WORK

As the SRAM bears the low-activity factor, several circuit level techniques have been reported by the researchers to address the low-leakage SRAM design as a major concern.

A. An Asymmetric SRAM Cell to Lower Gate Leakage

In [8], Azizi has proposed an asymmetric SRAM cell design in 70nm technology, Fig.3. In it an nMOS transistor is added to the SRAM bit-cell to reduce the magnitude of the gate voltage when the cell stores data '0', i.e., the cell is in the '0' state. In comparison with the conventional SRAM bit-cell, the gate leakage of the proposed structure decreases in the '0' state while it increases in the '1' state.

Also, the area and long access time are observed as penalty with no change in the dc noise margin (data storage integrity) in the design.

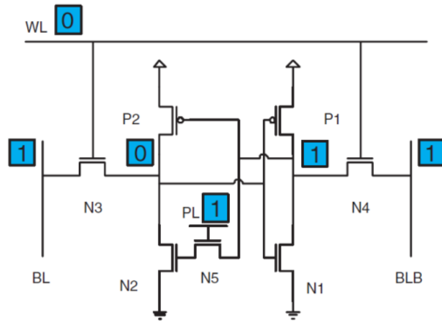


Fig.3: The Structure of Asymmetric Pass-Cell [8]

B. NC-SRAM Bit-Cell Design

Elakkumanan, in [9], has suggested the NC-SRAM design at 65nm technology and 0.8V, Fig. 4. It employs Dynamic Voltage Scaling (DVS) Scheme to reduce the leakage power of the SRAM bit-cells while retaining the stored data during the idle mode.

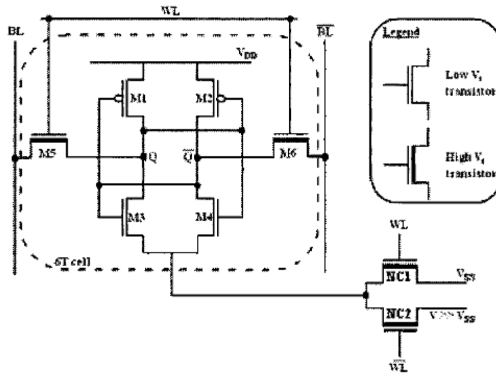


Fig.4. NC-SRAM Circuit: Pass Transistor Control Threshold Voltages of nMOS Transistors in the Cross-Coupled Inverter to Reduce the Leakage [9]

The key idea behind NC-SRAM is the use of two pass transistors NC1 and NC2 which provide different ground levels to the memory cell in the active and idle modes. The positive voltage (virtual ground) reduces the gate leakage and sub-threshold currents of the cell while degrading the read and write performances of the cell [9].

C. Dual-V_t SRAM Bit-Cell

Amelifard, in [10] has suggested a SRAM Bit-Cell topology using dual-gate oxide thicknesses in 65nm technology and at 1.0V supply voltage, Fig.5. It is another approach to reduce the gate leakage current in the SRAM cell [10]. In it, the gate oxide thicknesses of the nMOS pass transistors and the nMOS pull-down transistors are increased. Because the much lower gate leakage of pMOS transistor, no change is made to the gate oxide thickness of the pMOS pull-up transistors. To achieve a lower sub-threshold current, the dual threshold voltage technique has been used. The cell evaluation is performed by using the high threshold voltage for different transistors. In the best case, the power consumption is decreased and the stability is improved but the read access time is degraded [10].

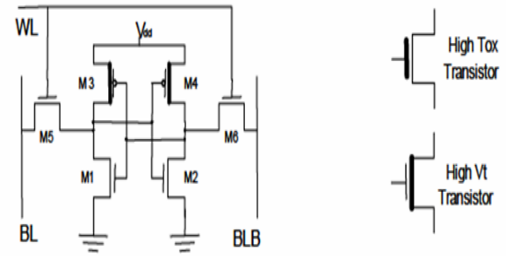


Fig. 5. Dual-V_t SRAM Bit-Cell Structure [10]

D. Gated-V_{DD} SRAM Bit-Cell

Ye, et.al., have proposed a circuit level technique as the name 'Gated-V_{DD}' [11] to gate the supply voltage and reduce the leakage power when the SRAM cells are in ideal mode with a minimal impact on performance, Fig.6. The sub-threshold leakage current and leakage energy dissipation increase exponentially with decreasing threshold voltage. Gated-V_{DD} "turn off" the supply voltage and eliminate virtually all the leakage energy dissipation in the cache's unused sections. The key idea is to introduce an extra transistor in the supply voltage (V_{DD}) or the ground path (GND) of the cache's SRAM cells. The extra transistor is turned ON in the used sections and turned OFF in the unused sections. Thus, the cell's supply voltage is "gated." Gated-V_{DD} maintains the performance advantages of lower supply and threshold voltages with reducing leakage power. The fundamental reason for the reduction in leakage is the stacking effect of self reverse-biasing of series-connected transistors [11]. Gated-V_{DD}'s extra transistor produces the stacking effect in conjunction with the SRAM cell transistors when the gated-V_{DD} transistor is turned off.

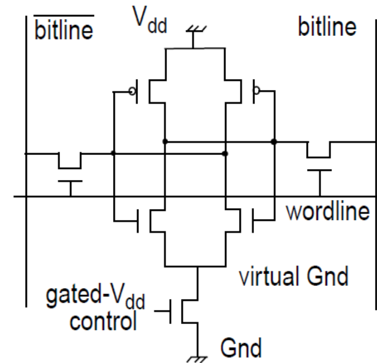


Fig. 6. SRAM with an NMOS Gated-V_{DD}

The role of the area overhead of the Gated Transistor is not much in case of a large cache as it is being used one transistor per row which is clear from Fig.7.

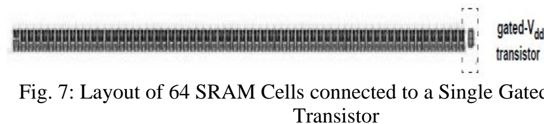


Fig. 7: Layout of 64 SRAM Cells connected to a Single Gated-V_{DD} nMOS Transistor

E. PP-SRAM Cell

G. Razavipour, et.al., in [3] have presented a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure, Fig.8., at 45nm technology and 0.8V supply voltage by giving a name to it as PP-SRAM Bit-Cell. It has lower gate leakage compared to that of the conventional SRAM cell. In order to decrease the gate leakage currents of the SRAM cell, nMOS pass transistors, are replaced by pMOS pass transistors P3 and P4. In the active mode, WL is held at '0' to turn ON the two pass transistors. In the idle mode, WL is charged to V_{DD}, so that the two pMOS pass transistors are OFF. Here, it is being pointed-out that due to the use of the pMOS transistors, there is an increase in the dynamic power of the cell which is consumed during the read and write operation. Also, since static power is much more important than dynamic power in large memories, static power saving will very well compensate for the increase in dynamic power dissipation [3].

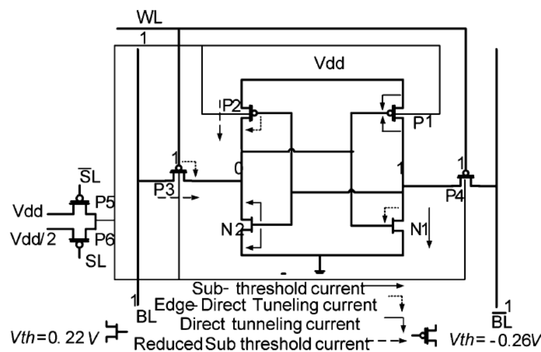


Fig.8. PP-SRAM Cell (Holding '0') with Gate Leakage Current [3]

In addition, the static power consumption induced by the two new inserted pMOS transistors (P5 and P6) is found to be small. The use of pMOS pass transistor, however, may lead to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of that of the nMOS for the technology used in this work [3].

IV. P4-SRAM BIT CELL - THE PROPOSED WORK

The proposed SRAM Bit-Cell called as P4-SRAM Bit-Cell is shown in Fig. 9. It mainly considers the fact that the barrier height of the holes is more than that of the electrons, i.e, 4.5eV vs 3.1eV, respectively. So, the gate leakage current will be lower in the off state of the pMOS transistors whereas the full-supply substrate body-bias will involve in the reduction of the sub-threshold leakage during the standby mode of the proposed design. This novel structure of SRAM Bit-Cell uses the concept of the transistor stacking for the leakage power reduction. The fundamental reason for the stacking in the leakage power reduction is the stacking effect of the self-reverse biasing of series connected transistors. To the best of my knowledge pMOS transistor stacking at the Gated-GND has been proposed for the first time at the 'full-supply voltage body-biasing' in the SRAM bit-cell. These, extra pMOS transistors of the Gated-GND, produces the stacking effect in conjunction with the SRAM Bit-Cell transistors when the Gated-GND transistors are turned-off by opposing flow of leakage current through them.

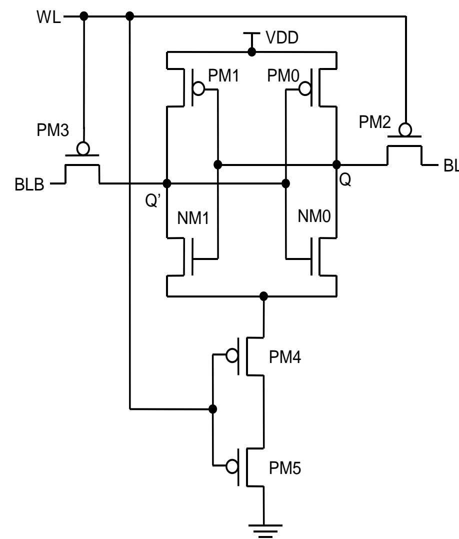


Fig.9. Proposed Novel P4-SRAM Bit-Cell Structure

When WL = '0', the bit-cell behaves as a normal conventional 6T bit-cell by turning the PM2 and PM3 transistors ON, i.e., cell is in the active state and is ready to write/read data. But when the WL = '1', the two access transistor (pMOS) are in OFF state. It also put both the stack pMOS transistors in the OFF state. To sink the current when the bit-cell is active (WL='0'), stacking transistors need to be ON. Hence, they are need to be made larger in size. But the too large gated-transistors may reduce the stacking effect. Also, bigger the size of the stacking transistors will improve the cell read time but will cost the area. It is a design trade-off and may be considered as per the application demanded. In the proposed design, in order to reduce the negative impact of threshold voltage on the speed of the bit-cell and to reduce the active power consumption, a forward full supply body-biasing is used in the pMOS transistors. In it, the body bias voltage of pMOS transistor in the idle mode and active mode is set to V_{DD}. This work used a single bias voltage (V_{DD}), it directly reduces the circuit complexity demands by the dynamic body bias technique [3]. It also reduces its area overhead. In this work, the external signal can be generated through the row decoder circuit is activated before the WL is activated for the read and write operations or can be applied through WL by assuring the proper write/read access time which further assures the reduction in the area and circuit complexity.

V. ANALYSIS AND SIMULATION WORK

A. Conventional 6T-CMOS SRAM Bit-Cell

Table 1: Power in Standby Mode of Operation – When Bit-Cell Hold Data '1'
Active Power in writing '1' is 4.011µW

Cell / Transistor	Power (W)
Conventional 6T Bit-Cell	9.128p
PD NM0	2.716p

PD NM1	882.2z
Pass Gate NM2	2.575p
Pass Gate NM3	2.085p
PU PM0	2.181a
PU PM1	1.751p

Table 2: Power in Standby Mode of Operation – When Bit-Cell Hold Data '0'
Active Power in writing '0' is 3.815µW

Cell / Transistor	Power (W)
Conventional 6T Bit-Cell	4.5p
PD NM0	25.1651f
PD NM1	2.717p
Pass Gate NM2	142.14z
Pass Gate NM3	3.277a
PU PM0	1.751p
PU PM1	6.57005f

B. Proposed SRAM Bit-Cell – P4 SRAM Bit-Cell

Table 3: Standby Mode of Operation – When Bit-Cell Hold Data '1'
Active Power in writing '1' is 418.65nW

Cell / Transistor	Power (W)
Proposed SRAM Bit-Cell	4.5235p
PD NM0	575.342f
PD NM1	1.3476p
Pass Gate PM2	2.5964p
Pass Gate PM3	458.49f
PU PM0	43.67a
PU PM1	337.6121f
Stack PM4	14.091f
Stack PM5	541.5f

Table 4: Standby Mode of Operation – When Bit-Cell Hold Data '0'
Active Power in writing '0' is 418.52nW

Cell / Transistor	Power (W)
Proposed SRAM Bit-Cell	2.435p
PD NM0	6.28892a
PD NM1	577.739f
Pass Gate PM2	962.3f
Pass Gate PM3	305.42z
PU PM0	338.94f
PU PM1	4.95228a
Stack PM4	14.343f
Stack PM5	541.9f

C. Analysis of Power Consumption – Active and Leakage

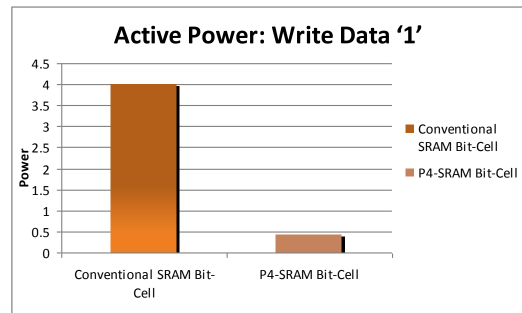


Fig.10: Active Power for Write Data '1'

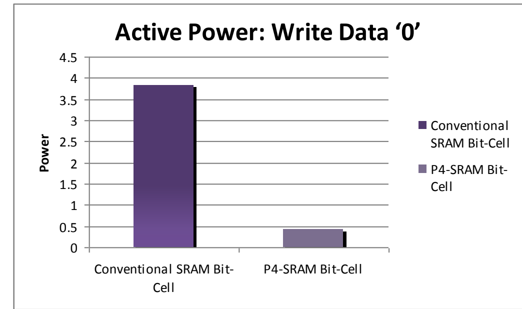


Fig.11: Active Power for Write Data '0'

The use of the pMOS transistors increases the dynamic power of the cell which is consumed during the read/write operations. In [3], considering the static power dissipation more important in large memory, the dynamic power has been compensated by the static power dissipation of the memory. Here, in the proposed work, we have reduced the dynamic power of the bit-cell by 89% for Write Data '0/1', individually, Table 1-4 and Fig. 10, 11.

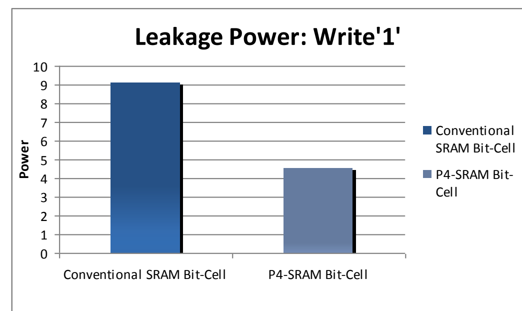


Fig.12: Leakage Power for Hold Data '1'

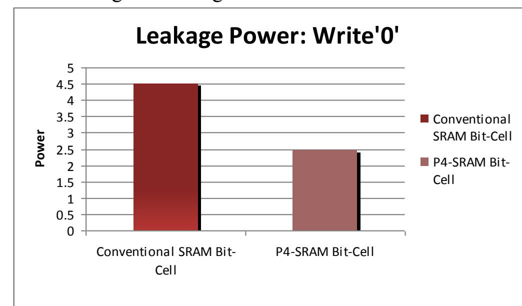


Fig.13: Leakage Power for Hold Data '0'

The leakage power consumption of the proposed P4-SRAM Bit-Cell is reduced by 50% while the cell is storing '1' and 46% when '0' at a small area penalty of two pMOS stack transistors, Table 1-4 and Fig. 12, 13.

The experimental results shows that the best power optimization is achieved at newly reported full-supply body bias of the pMOS transistors in the SRAM bit-cell, Table 5.

Table 5: Substrate Bias-Voltage vs Power Dissipation (Active & Leakage)

Bias Voltage (V)	Active Power (W)		Leakage Power (W)	
	Write Data '0'	Write Data '1'	Store Data '0'	Store Data '1'
0.7	418.52n	418.65n	2.4357p	2.4357p

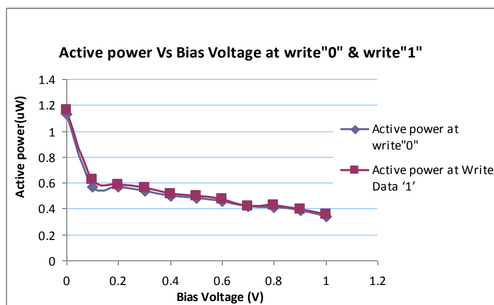


Fig.14: Active Power vs Substrate Bias Voltage for Data Write '0' and '1'

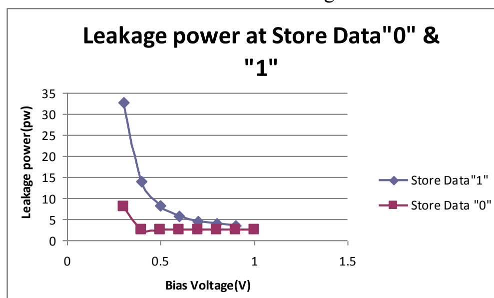


Fig.15: Leakage Power vs Substrate Bias Voltage for Data Hold '0' and '1'

This work utilizes the same body-bias voltage as the supply voltage V_{DD} is called as full-supply body biasing. It simplifies the need for complex dynamic body-bias voltage mechanism at different voltage levels and its control circuit. So that it may further supports area efficiency of the memory, Table 5, and Fig. 14, 15.

VI. CONCLUSIONS

In this paper, a novel structure of the SRAM Bit-Cell, called as P4-SRAM Bit-Cell structure, is presented. The proposed bit-cell utilizes the Gated-V_{DD} technique for transistor stacking in the PP-SRAM along with the full-supply body biasing to reduce the active, standby, and dynamic power in the memory. In comparison to the conventional 6T SRAM bit-cell, the total leakage power is reduced by 50% while the cell is storing data '1' and 46% when data '0' at a very small area penalty. The total active power reduction is achieved by 89% when cell is storing data 0 or 1. The design simulation work was performed on the deep-sub-micron CMOS technology, the 45nm, at 25^0C with V_{DD} of 0.7V for t_{OX} of 2.4nm.

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