

FPGA Implementation of 5/3 Integer DWT for Image Compression

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Abstract— The wavelet transform has emerged as a cutting edge technology, in the field of image compression. Wavelet-based coding provides substantial improvements in picture quality at higher compression ratios. In this paper an approach is proposed for the compression of an image using 5/3(lossless) Integer discrete wavelet transform (DWT) for Image Compression. The proposed architecture, based on new and fast lifting scheme approach for (5, 3) filter in DWT. Here an attempt is made to establish a Standard for a data compression algorithm applied to two-dimensional digital spatial image data from payload instruments.

Keywords-2D-DWT; Lifting; CCDS; wavelet transform; 1DDWT.

I. INTRODUCTION

The wavelet transform has gained widespread acceptance in signal processing in general and in image compression research in particular. In applications such as still image compression, Discrete Wavelet Transform (DWT) based schemes have outperformed other coding schemes like the ones based on Discrete Cosine Transform (DCT). The DWT has been introduced as a highly efficient and flexible method for sub band decomposition of signals. The two dimensional DWT (2D-DWT) is nowadays established as a key operation in image processing. This is due to the fact that DWT supports features like progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest, etc. In addition to image compression, the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target distinguishing and so forth.

The transform coding part utilizes Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT) and Discrete Wavelet Transform (DWT) etc. Most widely used and efficient compression scheme JPEG uses Discrete Cosine Transform in its transform coding part. It splits the whole image into 8X8 pixel blocks and then for each block DCT is applied. The DCT has the disadvantage of blocking artefacts (blurring of images at edges of the image blocks) at higher compression ratios. This is overcome by the use of Discrete Wavelet Transform, since it considers image as a whole and moreover, it does not have pre-processing of image (splitting it into 8X8 pixel blocks). Thus for the same quality of the output image DWT has better compression ratios.

DWT has traditionally been implemented by convolution. Such an implementation demands both a large number of

computations and a large storage—features that are not desirable for either high-speed or low-power applications. Recently, a lifting-based scheme that often requires far fewer computations has been proposed for the DWT [1].The transform coding part which we would be developing will be a 5/3 Integer Discrete Wavelet Transform (DWT). Suitable architecture is selected (lifting) [1] and the core is developed using VHDL.

II. CONSULTATIVE COMMITTEE FOR SPACE DATA SYSTEMS

The Consultative Committee for Space Data Systems (CCDS) is the recommendation for space data system standards. The main purpose of this paper is to establish a data compression algorithm applied to two-dimensional digital spatial image data from payload instruments based upon the recommendation [1].

III. LIFTING BASED DWT

The wavelet Lifting Scheme is a method for decomposing wavelet transforms into a set of stages. The convolution-based 1-D DWT requires both a large number of arithmetic computations and a large memory for storage. Such features are not desirable for either high speed or low-power image processing applications. The main feature of the lifting-based wavelet transform is to break-up the high pass and the low pass wavelet filters into a sequence of smaller filters. The lifting scheme requires fewer computations compared to the convolution-based DWT. Therefore the computational complexity is reduced to almost a half of those needed with a convolution approach [2][3].The Fig.1 illustrates Lifting Concept.

The main advantages of lifting scheme are as follows:

I) It allows a faster implementation of the wavelet transform.

II) The lifting scheme allows a fully in-place calculation of the wavelet transform. In other words, no auxiliary memory is needed and the original signal (image) can be replaced with its wavelet transform.

III) With the lifting scheme, the inverse wavelet transform can immediately be found by undoing the operations of the forward transform. In practice, this comes down to simply reversing the order of the operations and changing each + into a - and vice versa.

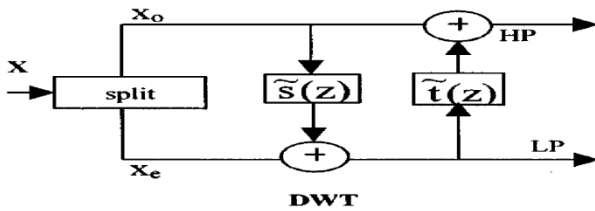


Fig. 1 Lifting Scheme

The three main steps of Lifting are

- a) *Predict* step: where the odd samples are multiplied by the time domain equivalent of $s(z)$ and are added to the even samples.
- b) *Update* step: where updated even samples are multiplied by the time domain equivalent of $t(z)$ and are added to the odd samples.
- c) *Scaling* step: where the even samples are multiplied by $1/K$ and odd samples by K .

A. Two-Dimensional Discrete Wavelet Transform

The basic idea of 2-D architecture is similar to 1-D architecture. A 2-D DWT can be seen as a 1-D wavelet transform along the rows and then a 1-D wavelet transform along the columns, as illustrated in Figure 2. The 2-DWT operates in a straightforward manner by inserting array transposition between the two 1-D DWT. The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands (see Fig.4) within the array defined by filter output. The LL sub-band represents an approximation of the original image, the LL1 sub-band can be considered as a 2:1 sub-sampled (both horizontally and vertically) version of the original image.

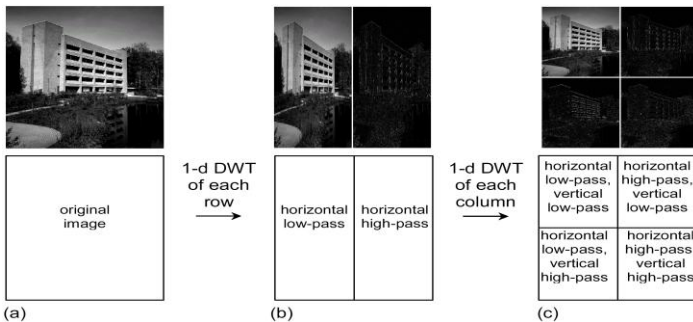


Fig. 2 2_d DWT(one level)

The other three sub-bands HL1, LH1, and HH1 contain higher frequency detail information (mostly local discontinuities in the edges of the image). This process is repeated for as many levels of decomposition as are desired.

Here level of decomposition is chosen as three. To increase compression effectiveness, correlation remaining in the LL sub band after the 2-d DWT decomposition is exploited by applying further levels of DWT decomposition to produce a

multi-level 2-d DWT (Fig.3). This produces the pyramidal decomposition [4].

CCSDS Recommendation standard specifies three level decomposition. As from the Figure.4 it is clear. Original Image undergoes first level decomposition to obtain four sub bands namely LL1, HL1, LH1, and HH1. Now the LL1 undergoes the second level decomposition to obtain the sub bands LL2, HL2, LH2 and HH2. In the final stage LL2 undergoes third level decomposition to obtain the sub bands LL3, HL3, LH3 and HH3. The DWT stage performs three levels of 2-D wavelet decomposition to obtain 10 sub bands as shown in the fig.4. Once LL1 undergoes first level decomposition remaining HL1, LH1 and HH1 are stored in DWT buffer as shown in fig 3. Similarly HL2, LH2 and HH2 are stored in buffer during next level decomposition. at each level of decomposition, the LL sub band from the previous level is decomposed, using a 2-d DWT, and is replaced with four new sub bands. Each new sub band is half the width and half the height of the LL sub band from which it was computed. Each additional level of decomposition thus increases the number of sub bands by three.

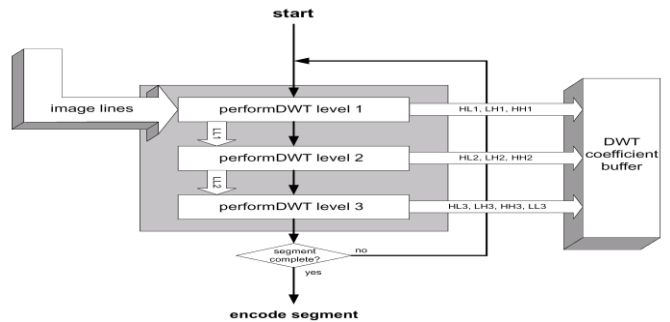


Fig.3 Program and Data Flow of DWT Module

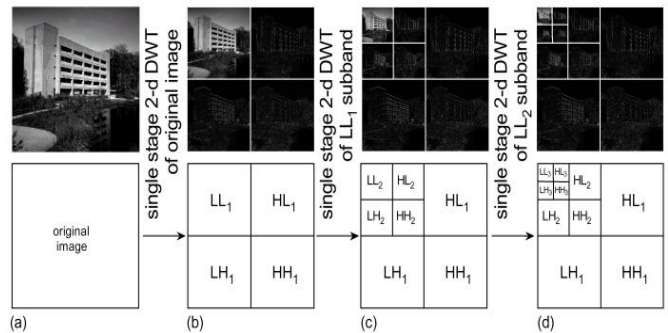


Fig. 4: Three-Level 2-d DWT Decomposition of a Image

IV. IMPLEMENTATION

CCSDS Recommended Standard use of a three-level, two dimensional (2-d), separable Discrete Wavelet Transform (DWT) with five and three taps for low- and high-pass filters, respectively. fig 5 shows the general schematic coder .

Two specific 1-d wavelets are specified with this Recommended Standard [1] Integer DWT which strictly supports lossless compression. Integer DWT is purely reversible i.e. reconstructed image will be same as original image.

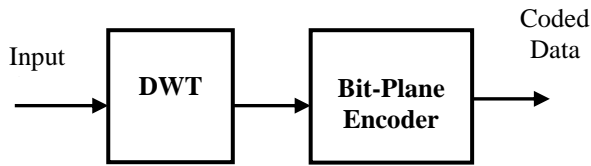


Fig .5 General Schematic of the coder

1-d Integer DWT maps a signal vector (shown in equation 1) to two sets of wavelet coefficients, one high-pass set, D_j , and one low pass set, C_j , in accordance with equations 2 and 3 [1] [2] [5]

For $N > 2$ let

$$\{X_0, X_1, \dots, X_{2N-1}\} \quad (1)$$

$$D_j = x_{2j+1} - \left\lfloor \frac{1}{2} (x_{2j}) + \frac{1}{2} (x_{2j+2}) \right\rfloor \quad (2)$$

For $j = 1 \dots N-3$

$$C_j = x_{2j} + \left\lfloor \frac{D_{2j-1} + D_{2j+1} + 2}{4} \right\rfloor \quad (3)$$

For $j = 1 \dots N-1$

Where “ $\lfloor \rfloor$ ” indicates floor brackets. Equations (2) and (3) define the integer transform that shall be used with this Recommended Standard. Given input values x_i , the D_j values in equation (2) shall be computed first and used subsequently to compute C_j values in equation (3). These equations are “Lifting Equations”.

A. Lifting Equations Implementation

The wavelet Lifting Scheme is a method for decomposing wavelet transforms into a set of stages. As compared to convolutional method the arithmetic computations required is less i.e computational complexity is reduced by half. Its implementation is described in fig.6

Forward transform

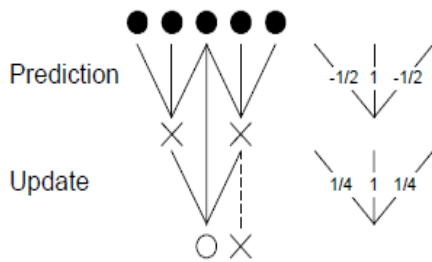


Fig .6 Lifting Concepts

The Figure .6 shows lifting concept where the odd samples are predicted from even samples which are called as prediction stage to obtain High Pass coefficients [6]. Then by using high Pass coefficients, Low Pass is updated which is the next step of lifting. Analysis of filter coefficients are shown in table no 1.

Table 1: Filter Coefficients for the 5/3 Integer DWT Filter

i	Low pass Filter h_i	High pass filter g_i
0	$3/4$	$1/2$
± 1	$1/4$	$-1/4$
± 2	$-1/8$	

V. VHDL IMPLEMENTATION

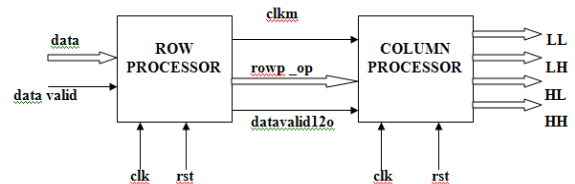


Fig .7.1 Block diagram for 1-level 2d-dwt

This is the basic block diagram for 1-level 2d-dwt which will produce the 1st level 4 sub bands, among them only LL band is used for the 2nd level dwt [7].

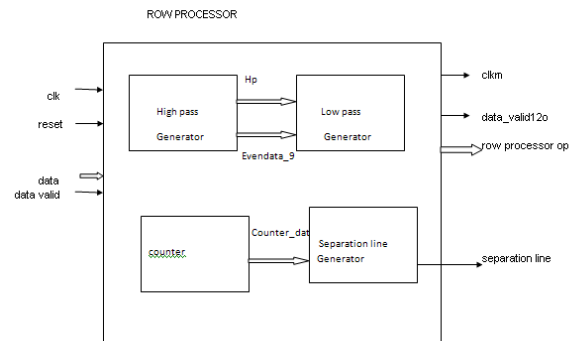


Fig 7.2 Block diagram of ROW processor

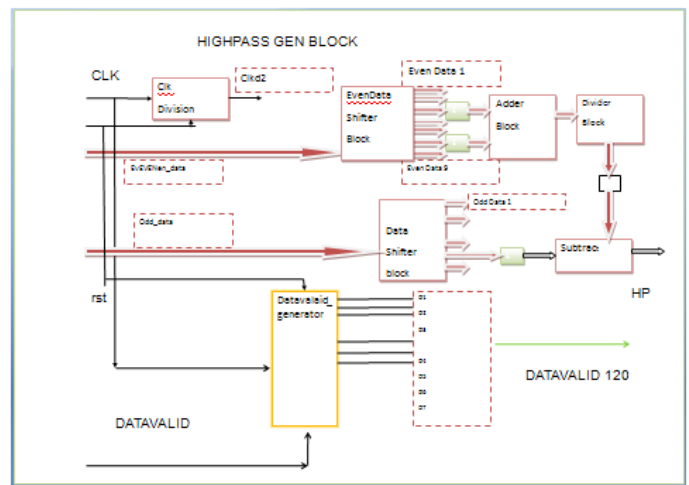


Fig 7.3 Block diagram of High pass generation block (ROW processor)

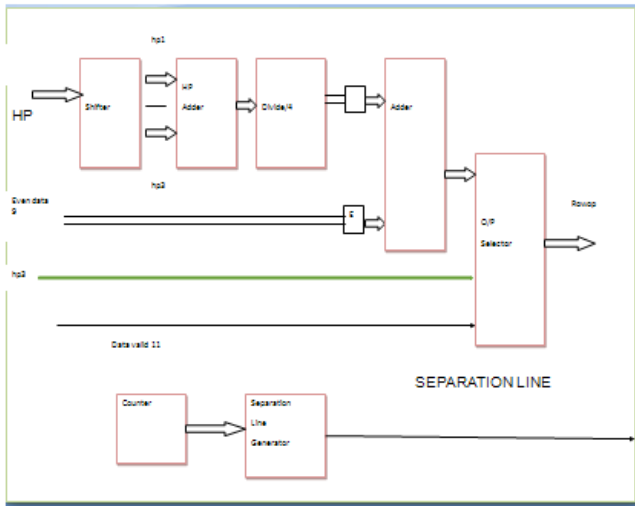


Fig 7.4 Block diagram of Low pass generation block (ROW processor)

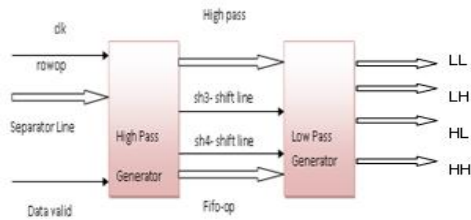


Fig 7.5 Block diagram of column processor

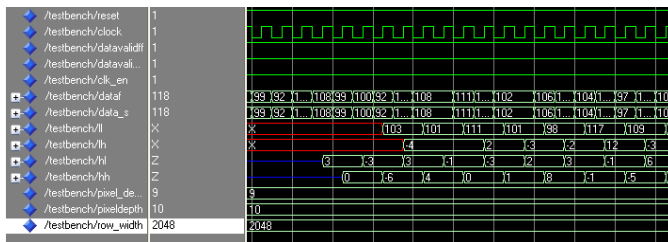


Fig 7.6 simulation results of 1 level 2d- DWT

VI. MEASURING OF PERFORMANCE

Mean Squared Error (MSE): MSE [1] is defined as follows:

$$MSE = \frac{1}{M} \sum_{i=1}^M (x_i - \hat{x}_i)^2$$

Where, M is the number of elements in the signal, or image. For example, if we wanted to find the MSE between the reconstructed and the original image, then we would take the difference between the two images pixel by pixel, square the results, and average the results. Peak Signal to Noise Ratio (PSNR): The PSNR [1] is defined as follows:

$$PSNR = 10 \log_{10} \left(\frac{(2^n - 1)^2}{MSE} \right)$$

Where, n is the number of bits per symbol. As an example, if we want to find the PSNR between two 256 gray level images, then we set n to 8 bits. The following table no 3 give the psnr and rms calculation done for the 128×128 size of different images

Table 2: performance measures results for 1 level 2D DWT (with flooring and ceiling function)

Image	Avg error	RMS error	PSNR	SNR
Lenna	0.0	0.0	infinity	infinity
Baboon	0.0	0.0	infinity	infinity
Peppers	0.0	0.0	infinity	infinity
cameraman	0.0	0.0	infinity	infinity
goldhill	0.0	0.0	infinity	infinity

VII. RESULTS AND OBSERVATION



Fig.8.1 vhdl row processor output



Fig .8.2 column processor output.



Fig.9 Three –Level decomposition of Lena Image using C++ code.

The DWT level chosen is one for FPGA implementation in this paper.

VIII. CONCLUSION

In this paper, an approach is made proposed architecture for the $5/3$ Integer 2D-DWT to meet the requirements of real-time image processing. As mentioned in CCSDS document for three level decomposition of $9/7$ Integer DWT is used to implement $5/3$ filter.

The proposed architecture has been correctly verified by writing the code using VHDL Language. The code is synthesized using Axcelerator FPGA family. The estimated frequency of operation is around 60MHz.

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