Energy-Aware Fragmented Memory Architecture with a Switching Power Supply for Sensor Node

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***Abstract*—The basic sensor node architecture in a wireless sensor network contains sensing, transceiver, processing and memory units along with the power supply module. Because the basic sensor network application nature is surveillance, these networks may be deployed in a remote environment without human intervention. The sensor nodes are also battery-powered tiny devices with limited memory capacity. Because of these sensor node limitations, the architecture can be modified to efficiently utilise energy during memory accesses by dividing the memory into multiple banks and including a memory switching controller unit and a power switching module. This modification conserves energy, so power can be supplied only to the bank or part of the memory being accessed instead of powering the entire memory module, thus leading to efficient energy consumption. Simulations have been performed on fragmented memory architecture by incorporating the M/M/1 queuing model. When the packets get queued up, energy utilisation and a packet drop at the sensor node is observed. The energy consumption is reduced by an average of 70%, and there is significantly less packet drop compared to the normal memory architecture. This leads to increase in node and network lifetime and prevents information loss.**

Keywords—modified memory architecture; switching power supply; sensor node; energy conserve; idle energy

I. Introduction

A wireless sensor network is an essential networking component in applications, including fire surveillance, underwater experiments and robotic flying sensors. Wireless sensor networks contain sensor nodes, where each sensor node has sensing, transceiver, processing and memory units, as in figure 1.The limited memory capability and energy utilisation nature of the sensor nodes has compelled many researchers to explore this area. The memory architecture of a sensor node usually has RAM with less memory capacity, which is used to store programs for processing (32 KB – 128 KB). Modern flash-based micro-controllers contain between 1 KB and 512 KB of memory for program storage. This can be used as both program memory and for temporary data storage.

The flash memory design influences the sensor node life span. Flash memory has recently become a popular alternative storage for many portable devices. Constructing memory architecture in a wireless sensor network depends on the application type. The traffic data size also varies from small to large based on the application.

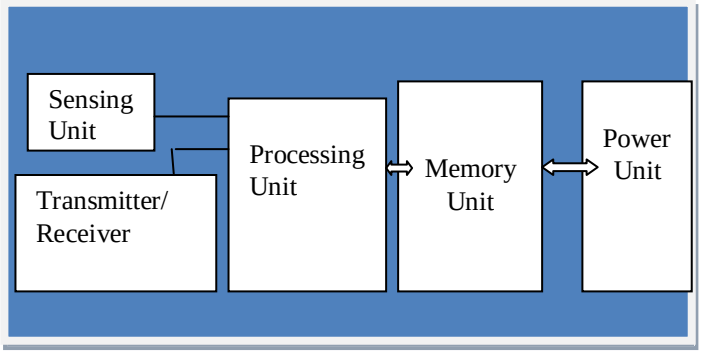

Fig.1. A typical Wireless Sensor Node

Transmitting scalar data, e.g., temperature, humidity or pressure, resort to a smaller traffic size over the WSN; transmitting captured images, videos or audio requires more information to be sent over the WSN. When the sensor nodes are deployed for a specific application within the network and are switched on, power is also supplied to the memory unit attached to the nodes even if the sensors are idle. The energy consumed in this state is known as idle energy, as the sensor is not performing any useful operation. There is thus a need to modify the sensor node architecture by incorporating efficient memory or buffer management schemes.

II. Literature Survey

The following section gives an insight into the work performed in this direction. The paper titled “Reducing Power Consumption for Mobile Multimedia Handsets” by authors Rong-Jaye Chen, Ting-Yu Lin, and Yi-Bing Lin [1] proposes 3 techniques called wake-up techniques that reduce battery power consumption in a mobile multimedia handset. Using these approaches, the system switches to sleep mode when the memory queue for packet arrivals is empty. Various wake-up mechanisms are considered based on these concepts. First among the approaches is the threshold approach mechanism. If the number of packets that have arrived in the memory queue is above a threshold, the system is switched on; otherwise, it remains in sleep mode. The second approach, called the vacation approach, switches on the system after completing vacation time. The third approach, called the hybrid approach, combines the above two approaches. In this approach, the system is turned on when either the memory queue length goes over the threshold level or at the end of vacation time. A comparative study of these approaches sheds light on some

important system performance parameters. The threshold approach also reduces the system switch-on rate, whereas the vacation approach has the lowest mean packet waiting time. The hybrid approach must he selected to maintain lower values for both the system switch-on rate and the mean packet waiting time. There is a possibility to obtain a set of threshold values and determine a small switch-on rate and the probability for packet dropping for a threshold approach, while such a possibility does not exist for the vacation approach to obtain the vacation time range.

The authors Tie Qiu, Lin Feng, Feng Xia, Guowei Wu, and Yu Zhou have published a paper titled "A Packet Buffer Evaluation Method Exploiting Queuing Theory for Wireless Sensor Networks". They focus on optimising the performance of a large-scale wireless sensor network for improved QoS transmission when the hardware consumption is limited. Their paper [2] proposes a novel evaluation scheme based on the packet buffer capacity of nodes using a queuing network model. The packet buffer capacity parameter for the queue is analysed for each node type when it is in the best working condition. This method expands the queuing network model into the equivalent queuing network model by adding holding nodes to the existing network to evaluate congestion within the queuing network and obtain effective arrival and transmission rates. This work establishes an M/M/1/N-type open queuing network model with WSN holding nodes; it includes designing approximate iterative algorithms to calculate arrival rates when the system reaches a steady state. Experimental results indicate that the model is consistent with real-world data. This paper discusses modelling for only a single-server WSN model and proposes a method to calculate the packet buffer capacity size for nodes. Recent research focuses on the convergence of multiple processor nodes that can be used for M/M/m/N queues, which are also multi-server queues. For large-scale WSNs, prioritised clusters can effectively improve WSN performance, which will be our follow-up research.

In the paper "Fundamental Lower Bound for Node Buffer Size in Intermittently connected Wireless Networks", the author analyse the fundamental lower bound for the node buffer size in intermittently connected wireless networks. Due to some external constraints, there is a possibility that node inactivity may occur, which is the main cause for intermittent network connectivity. In a static random network, each node keeps a constant message generation rate. The buffer occupation in each node does not approach zero despite having infinite network capacity and node processing speed. A detailed analysis has been performed on buffer occupation when the channel capacity is infinite, and the results can be viewed as a lower bound for networks with finite channel capacity. The analysis show that when the probability of node inactivity is below the critical value, the network state is supercritical, and the fundamental achievable lower bound of the node buffer size is $\Theta(1)$. The minimum node buffer size requirements are asymptotically independent of network size, and when the probability of node inactivity is greater than the critical value, the network state is subcritical and the achievable lower bound on node buffer size shoots up as the network expands in the order of $\Theta(\sqrt{n})$.

The paper "Limiting the Power Consumption of Main Memory" focuses [4][5] on the peak power consumption by the hardware components. This affects the power supply, packaging and cooling requirements of the system's hardware. Higher peak power consumption by the hardware leads to bulky and expensive systems. If the components and systems actually require peak power, it becomes necessary to limit the power consumption to a less-than-peak power budget. This leads to intelligent provisioning of the power supplies, packaging and cooling infrastructures for the hardware components. This paper studies dynamic approaches to limit the power consumption by the main memories. It proposes 4 techniques, i.e., Knapsack, LRU-Greedy, LRU-Smooth, and LRU-Ordered, in which the memory device power state are adjusted as a function of load on the memory subsystem. The simulations carried out from 3 benchmark applications prove that these techniques consistently limit the power to a pre-established budget accompanied by low performance degradation. The simulation results indicate that limiting power using these techniques has the same effect as the conservation approach used in state-of-the-art techniques exclusively designed for performance-aware energy management. Limitations of this work include addressing issues related to selecting an ideal power budget in different scenarios and studying the effect of greater concurrency in memory accesses in the context of chip multiprocessors in future.

Han-Lin Li, Chia-Lin Yang, and Hung-Wei Tseng have presented a paper titled "Energy-Aware Flash Memory Management in Virtual Memory System", which revisits the design of virtual memory system using flash memory [7][8][9] for many portable devices due to its improvements in storage capacity, reliability and lower power consumption. This paper concentrates on the energy efficiency aspect, as power is the first-order design consideration for embedded systems. Frequent writes into the flash memory lead to frequent garbage collection, thus incurring significant energy overhead. This is due to the write-once feature of the flash memory. To address this issue in increased energy consumption and prevent excess energy lost, the authors have proposed 3 methods to reduce the number of writes occurring in the flash memory. They are HotCache scheme, Subpaging technique and Duplication-aware garbage collection method. In the HotCache scheme, an SRAM cache is introduced to buffer frequent writes. In the subpaging technique, pages are partitioned into subunits and only dirty pages are written into the flash memory when a page fault occurs. The duplication-aware garbage collection method uses the data redundancy that exists between the flash and main memory to bring reduction in the writings that occur due to garbage collection. Intrapage locality, a type of data locality, is an inherent feature of flash memory and responsible for data allocation. This property of the flash memory should be carefully preserved while data are written from the storage buffer to flash memory. Destroying this property leads to increase in the energy consumption by the flash memory. Experiments have been performed using the 3 techniques and the results show an average energy reduction of 42.2% using the combination of the 3 techniques.

Several papers [11] [12] [13] address the basic issues involved in architectural design and the S used in sensor network applications. These papers present open issues in the hardware design and software components in wireless/multimedia sensor networks. Authors also classified the off-the-shelf hardware and the research prototype currently used in different forms sensor network. Much research has been performed in cluster–based WSN, focusing on energy efficiency and scalability related to clustering protocols. To select the cluster head in statistical techniques [14], all sensor nodes in the network equally share the role of cluster head, which adds to the life span of the sensor node. The HEED Clustering algorithm [15] implements a hybrid model to select the cluster head based on the residual energy of the node and its proximity to its neighbours - an additional parameter involved the selection process. The issues related to the power of balanced energy consumption among the cluster head nodes have been discussed in [16, 17]. The ACE clustering algorithm [18] partitions a network into uniformly dispersed clusters. Another clustering technique known as autonomous clustering and uses the coverage estimation parameter [19][20][21].

III. Memory Bank Architecture for a Wireless Sensor Node

In the heterogeneous network class, wireless sensor networks form the lower level of the Internet networking hierarchy, where energy utilisation due to various factors is the main issue that affects the lifespan of the wireless sensor network and must be considered during the design of the network architecture. One such energy-consuming factor is the memory access operations. Figure 2 shows the block diagram shows the modified sensor node along with Figure 3 modified memory architecture with switching power controller unit. Consider 128 KB flash memory that is equally divided into 4 blocks of 32 KB each and are known as memory banks. The architecture also contains a memory switching controller unit that will select the memory block and amount of memory needed by the sensor node based on the traffic flow. This leads to energy conservation by the memory unit in the sensor node where only that part of memory that is currently in use is powered.

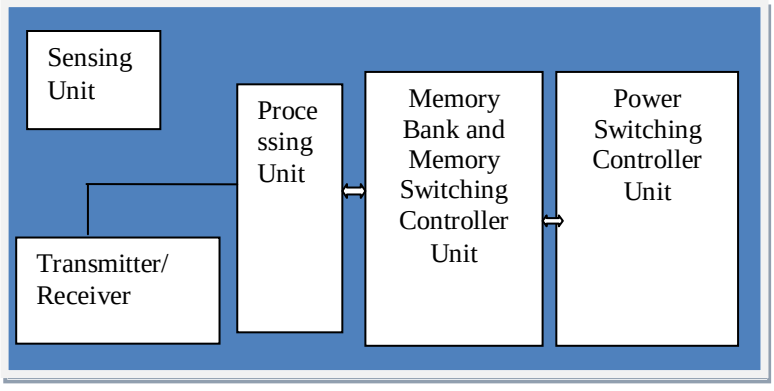

Fig.2. A typical Modified Wireless Sensor Node

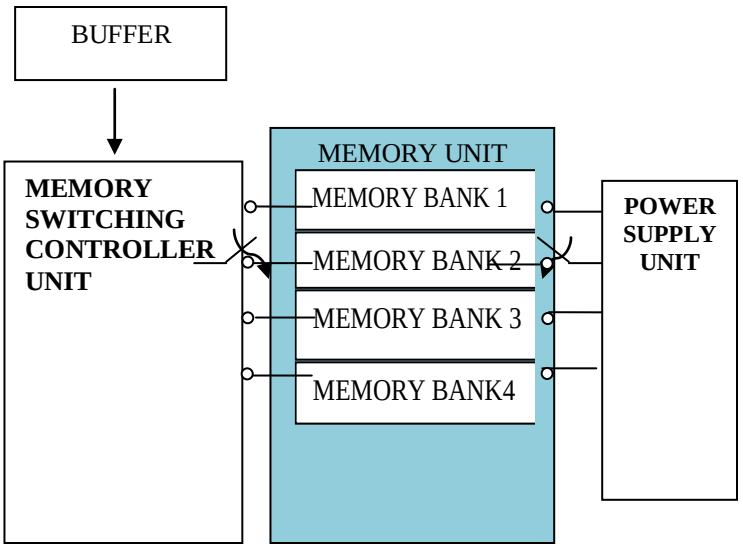

Fig.3. Block Diagram of Memory Bank Architecture of a Sensor Node

The amount of traffic flow is application-specific. Let us consider Aibe is following cues…

es.

Case I: Within the WSN, there are sensors that sense data, including temperature, humidity, and pressure. Such data require less storage.

Case II: WSN may also comprise multimedia sensors that capture multimedia information, such as images, video or audio, and process them. Processing of such data may include decision making, which is performed by the intelligent systems in the network. In such cases, the multimedia information requires large amounts of storage.

It is thus up to the sensor node to activate the number of memory banks required in the system based on the application for optimised energy utilisation.

In most wireless sensor network applications, we find variations in the traffic flow i.e., for some duration of the network operation the traffic flow is increased, while at some time the traffic flow is decreased. Thus an optimised way to achieve energy consumption is to divide the memory into a number of blocks and then use (power) only the part of the memory required for data storage. For example, let us say that amount of storage required for storing the data sensed by the node is only 20 KB out of total flash memory size of 256 KB. One approach is to consider the whole memory of 256 KB as one block and use only 20 KB. Though only 20 KB of space is being utilised but the power is supplied to the entire 256 KB memory. There is unnecessary wastage of excessive power in such a scenario, and this wastage can be avoided. Another alternative is to consider the memory unit consisting of a switching controller unit and divide the 256 KB memory into 8 banks of 32 KB each and use only 1 memory bank to store 20 KB of data; i.e., power is supplied to only 1 memory bank by the switching controller unit and the remaining 7 banks are switched off. Because less memory is being utilised, the power required will also be reduced thus leading to the

conservation of energy utilisation by the memory unit in the sensor node. The power consumption in different scenarios is given as follows:

Normal Scenario 1: power consumption in normal memory architecture as shown in FIG. 4

P_{normal} =Energy Dissipation (i.e., P_{read},P_{write}, $P_{process}$)for usage space + Idle Energy

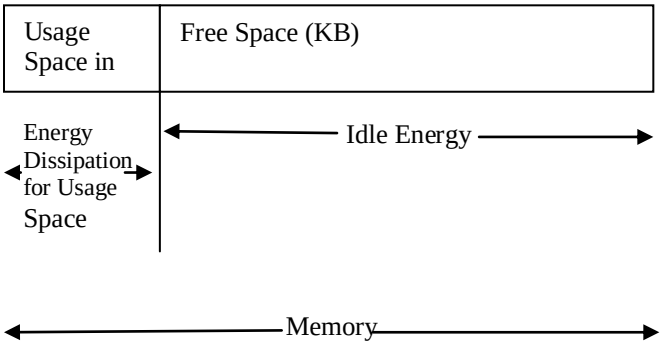

Fig.4. Energy Dissipation in normal memory architecture

Modified Scenario 2: power consumption in modified memory architecture from figure 5

P= {Number of Memory Bank} X Energy Dissipation (i.e., P_{read}, P_{write}, $P_{process}$)

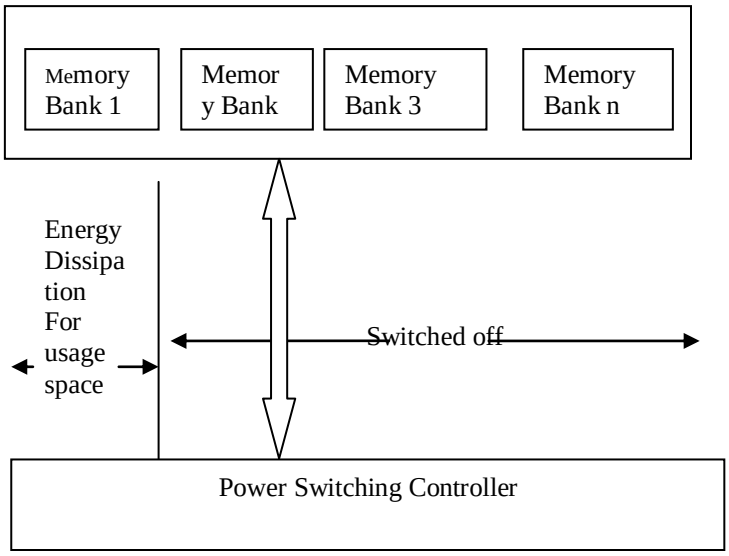

Fig.5. Energy dissipation in modified memory architecture

Figure 5 shows that ideal energy dissipation can be minimised, which conserves energy and leads to increases in the node lifetime.

IV. System Model for Memory Architecture

We have considered a simple queue system model in which packets arrive according to Poisson's model at rate λ, so the interarrival times are independent exponential random variable switch mean 1/ λ. In an M/M/1 model [10], the packet distribution is Poisson with rate λ or the interarrival time distribution is exponential using mean time 1/λ. Similarly, the service rate distribution is also based on a Poisson model with rate μ or is exponential with the mean time 1/μ. Interarrival and service times are independent variables. Assume that four packets, P_1 through P_4, arrive randomly and require service time S_1 through S_4. E_a is the energy dissipation for receiving the packet, E_s is energy dissipated during servicing the packet and E_q is energy dissipation when the packet is in queue, as in figure 6.

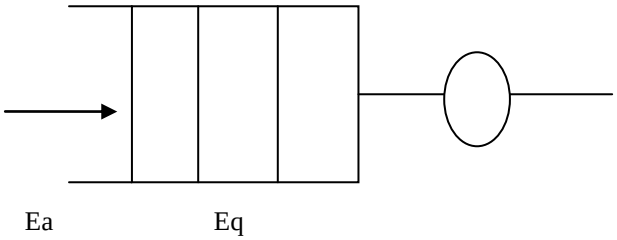

Fig.6. . Queuing Model

A. *Algorithm for modified memory architecture*

Input data:
$P_1,P_2,P_3 \ldots P_n$: Arriving Packets
$S_1,S_2,S_3 \ldots S_n$: Service Time for every Packet
Ea : Energy Dissipation for packet arrival
Es : Energy Dissipation for servicing the packet
Eq : Energy dissipation for queuing or Storing in buffer
n : Number of memory banks in use

Step 1: Traffic is generated i.e., interarrival and service times are generated using random processes for all incoming packets.
Step 2: if server is idle then
Packet is serviced
Else
Based on memory requirement by the arriving packets, memory banks are allocated by the memory controller and power switching controller unit will supply power to only the allocated memory banks.

Packet is stored in queue

End if

Total Energy Consumption = Ea + n* Eq +Es

Step 3: END

V. Simulation Environment:

We have considered the M/M/1 model to generate the traffic flow at the sensor nodes. In this process, the interarrival and service times are generated randomly using a Poisson distribution, and the total energy consumption is calculated for every event occurring in the sensor node. The analysis has been performed, varying both interarrival and service times. Figure 7 provides a sample snapshot with a graphical user interface created for the simulation.

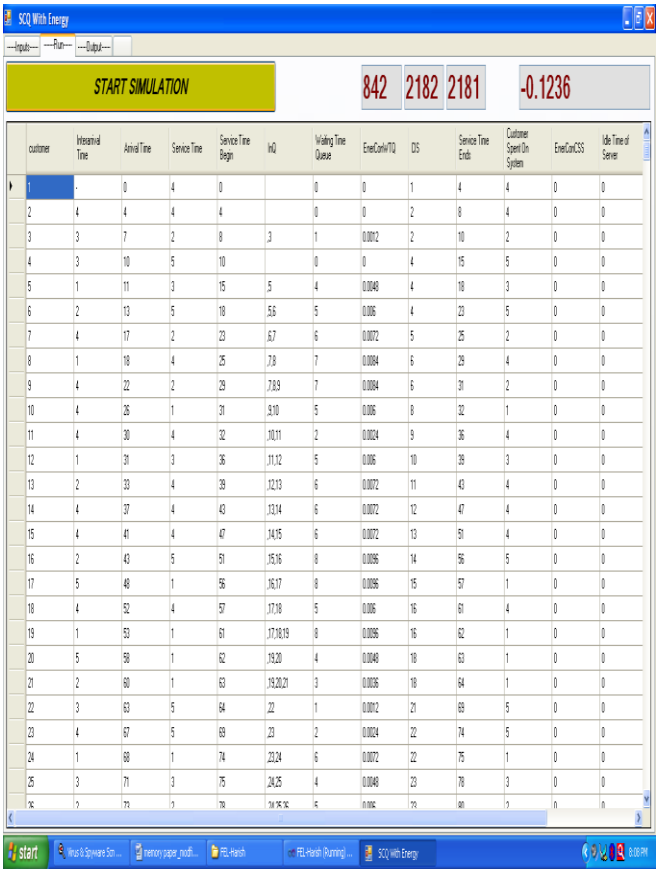

Fig.7. GUI Snapshot

VI. Result Analysis

In this section, we present the results obtained from simulations.

Table I lists the parameters and their corresponding values considered in the simulations.

Table I. Simulation Parameters:

Parameters	Value
Energy Threshold	200 Joules
Energy for Receiving	0.057 Joules
Energy for Transmitting	0.033 Joules
Idle Queue Energy	0.00012 Joules
Interarrival Time	1-7 sec
Service Time	1-7 sec
Number of Packets	1000 Packets
Queue Length	100 Packets

The graphs in Figures 8 - 10 are the plots of Service time (sec) on the X-axis and Energy Consumption (Joules) on the Y-axis.

Case I: Interarrival time: 1 sec
Service time : 1-5 sec

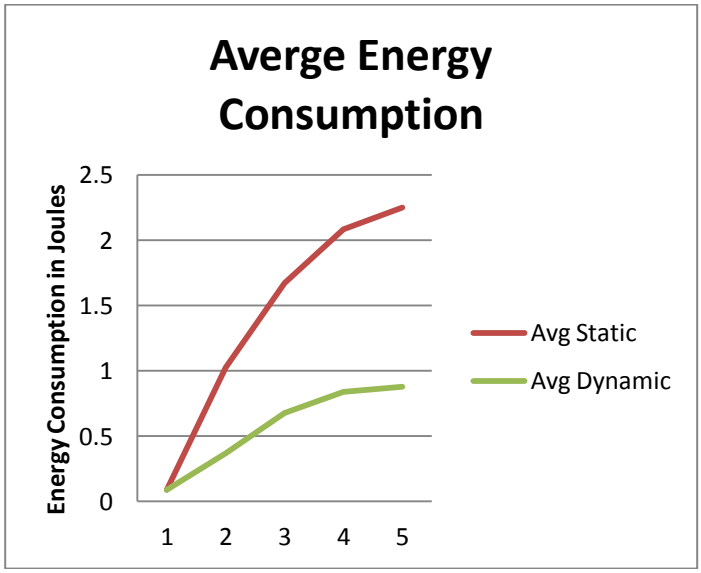

Fig.8. Comparing the average energy consumption normal memory (static) with modified memory architecture (Dynamic) for an interarrival time of 1 sec

Figure 8 shows that at service time 1 sec, there is a deviation in the energy utilisation curve for a memory-modified architecture (green curve) from the energy utilisation curve obtained for the normal memory architecture (red curve) without the memory banks. The energy utilisation by the modified architecture is significantly less than that of the normal architecture.

Case II: Interarrival time: 1-2 sec
Service Time: 1-5 sec

Figure 9 shows that the energy utilisation curves for both architectures are almost the same. At 2 sec of service time, the deviation occurs, i.e., the energy consumed during the memory operations in the normal memory architecture are much more than the modified memory architecture at the node.

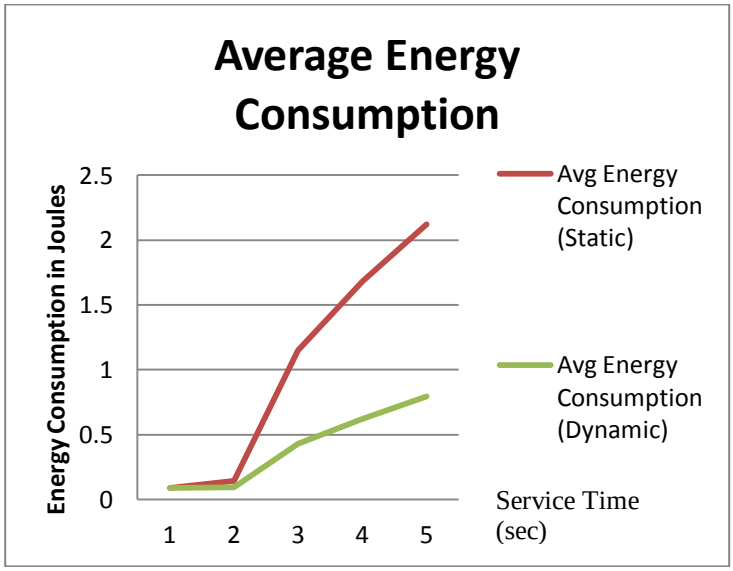

Fig.9. Comparison of average energy consumption normal memory(static) with modified memory architecture (Dynamic) for interarrival time between 1 -2 sec

Case III: Interarrival time: 1-5sec
Service time : 1- 5sec

Figure 10. Energy conservation is achieved using modified memory architecture.

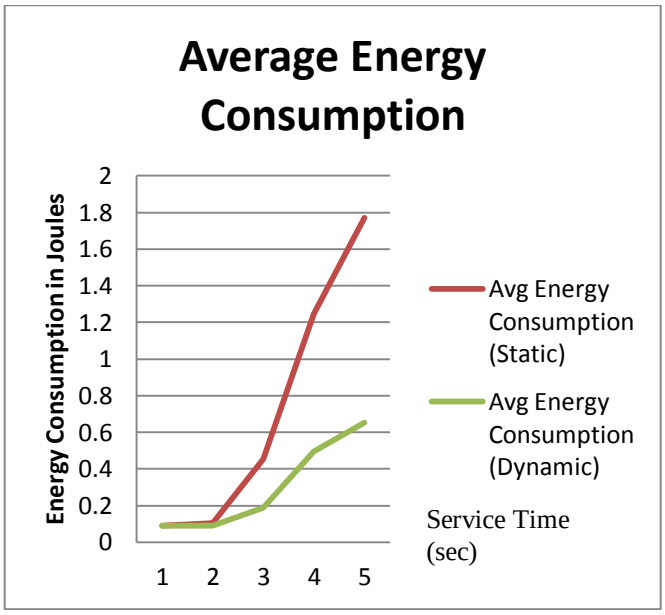

Fig.10. Comparing average energy consumption normal memory (static) with modified memory architecture (Dynamic); interarrival times between 1 and 5 sec

From Case-I to Case-III, the energy utilisation curve for the modified memory architecture clearly deviates from the normal curve. The energy consumed in the dynamic method is much lower than the original node memory architecture. During the simulations, this deviation occurs because the modified memory architecture increases in performance over the normal architect, as more packets get queued up to be serviced in the sensor node by consuming less energy during memory operations, which leads to energy saving and thus increases the network lifetime.

The graphs in Figures 11 to 13 plot of Service time (sec) on X-axis vs. Number of Packets dropped on Y-axis.

Case IV: Interarrival time: 1 sec
Service time: 1-5 sec
Case V: Interarrival time: 1-2 sec
Service Time: 1-5 sec
Case VI: Interarrival time: 1-5sec
Service time: 1-5sec

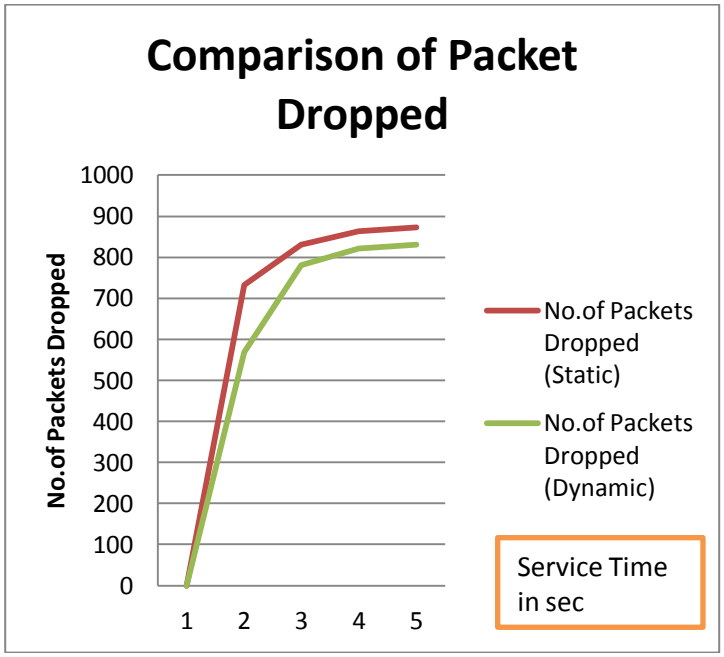

Fig.11. Comparing the number of packets dropped in normal memory (static) with modified memory architecture (Dynamic) with interarival time 1 sec.

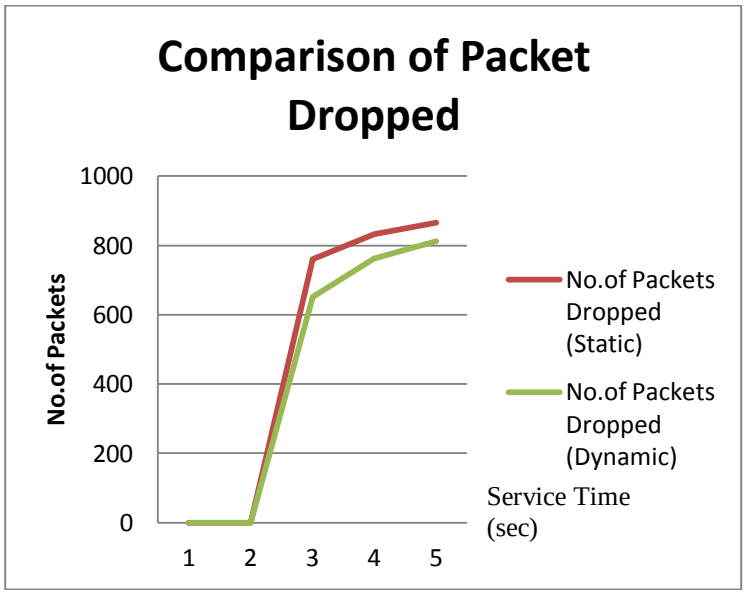

Fig.12. Comparing the number of packets dropped in normal memory (static) with a modified memory architecture (Dynamic) with interarrival between 1 and 2 sec

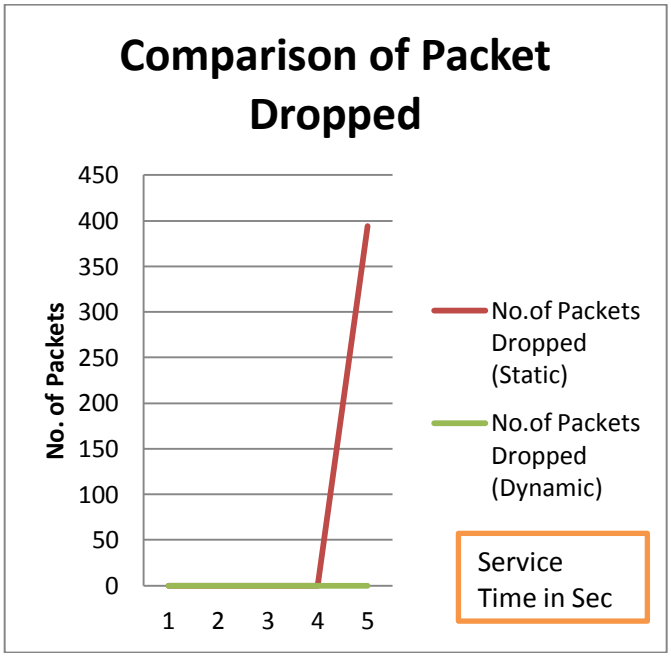

Fig.13. Comparing the number of packets dropped in normal memory (static) with modified memory architecture (Dynamic) with interarrival between 1 and 5sec

From Case-IV to Case-VI, the packet dropped in the dynamic method is less than the original node memory architecture. During the simulations, a variation in packet arrival is observed, i.e., interarrival time, where more packets get queued up to be serviced and the modified memory architecture show less packet drop in performance as against the normal architecture.

VII. Conclusion

This work proposes a modification of the memory architecture in the sensor node. In this architecture, the memory module is divided into several blocks known as memory banks that are activated by the memory controller unit and power-switching module. Depending on the amount of traffic flow the memory banks are activated. Simulations have been performed for varying interarrival and service times using the M/M/1 queuing model.

The graphs and simulations show a small difference in the energy utilisation at the initial stages when there are fewer packets in the queue and the service time is low. As the number of packets getting queued up and service time increase, the modified memory architecture performs significantly better than the normal memory architecture, considering the performance parameters energy consumption and packet drop. This increases the node lifetime and network lifetime.

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