A Conversion of Empirical MOS Transistor Model Extracted from 180 nm Technology to EKV3.0 Model using MATLAB

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***Abstract*—In this paper, the EKV3.0 model used for RF analog designs was validated in all-inversion regions under bias conditions and geometrical effects. A conversion of empirical data of 180nm CMOS process to EKV model was proposed. A MATLAB developed algorithm for parameter extraction was set up to evaluate the basic EKV model parameters. Respecting the substrate, and as long as the source and drain voltages remain constant, the DC currents and g_m/I_D real transistors ratio can be reconstructed by means of the EKV model with acceptable accuracy even with short channel devices. The results verify that the model takes into account the second order effects such as DIBL and CLM. The sizing of the elementary amplifier was considered in the studied example. The sizing procedure based on g_m/I_D methodology was described considering a semi-empirical model and an EKV model. The two gave close results.**

***Keywords*—EKV model; g_m/I_D methodology; analog design; MATLAB**

I. Introduction

Developing high performance low-voltage analog circuits is required for implantable biomedical devices and portative systems. Several attempts have been made proposing some MOS models and analog circuit design methodologies. The MOS transistors modelling for analog integrated circuit and RF design has to extremely precise to predict correctly the behaviour of a real transistor and cover all the transistor operation regions.

The PSP model [1] is surface-potential-based considered as the most recent advanced MOSFET model. It was even selected by Compact Model Council as the new industry standard MOSFET model aimed to replace the BSIM3/4 for the advanced CMOS designs. It includes all the essential effects in the state of the art MOS transistors from the effects of the reverse short-channel to the long channel degradation. Although the PSP is very instrumental for the understanding of the MOS transistors operation modes, it is not suited for a circuit design: The PSP model relies on an explicit formulation of the potential of surface according to the terminal voltage of the MOS device. The analog circuit setting equations according to a PSP model is difficult. This paper opted, therefore; for a PSP model rather than a dimensioning tool. Enz, Krumenacher and Vittoz [2] [3] as well as others [4] respectively suggested the EKV model and ACM models which were specially developed for this purpose. They were derived from the gradual channel approximation. As for [2] [5], they proposed more advanced versions considering short channel effects and mobility degradation.

The basic notions of the E.K.V3 model were reviewed in this paper. In fact the charge-based compact EKV3 MOSFET model is an analog/RF IC design tool. The first versions of this compact model used an empirical current-voltage relationship [6] to address the moderate inversion successfully. It was pioneer in adopting a substrate instead of source, and exploiting the symmetrical forward-reverse operation of MOS transistors [7]. A design methodology based on the level of inversion (or inversion coefficient, IC) was developed by [8]. The developed EKV3 model [9] included several other specificities for non-quasi static (NQS) operation [10], RF operation [11], NQS thermal noise [12] and handling of short-thermal noise [13]. Further details on EKV3 may be found in [14] [15].

The EKV model led to the development of a ratio-based design technique known the gm/ I_D based methodology intended for low-power analog circuits. In such circuits the moderate-inversion region is often applied as it allows a good compromise between speed and power consumption [5][16][17]. The g_m/I_D sizing methodology was first introduced in [18]. Since then, the concept has been referenced by many publications [19] [20].

The ACM model has also led to the development of the g_m/I_D based Methodology [5] [21]. According to the above mentioned models, the gm/I_D based methodology using the characteristic of g_m/I_D as a function of the normalized current diagram is very useful from the point of view power and speed for the analog circuit design.

II. Motivation and Organisation of the Work

The success of RF design depends heavily on transistor modeling. This requires efficient and compact models for the active and passive circuit elements. Since the MOS transistor is the essential circuit element, great effort has been made to model its DC and AC behavior accurately. Furthermore designing a circuit for electronic systems with reduced power consumption is the ultimate purpose of any circuit designer. For this low power design, it is vital to use low voltage and low current circuits. This means that MOSFETs can operate in the weak or moderate inversion region in the low power circuit.

The motive behind this work was to develop an EKV 3.0 model for 180nm TSMC technology with few numbers of parameters which allow precise designs in all-inversion regions of MOS transistor. This modeling would provide flexibility and optimal sizing for analog RF designers using 180nm TSMC technology.

The aim of this compact model was to obtain simple, fast, and accurate representations of the device behavior. This paper tried to validate the EKV model according to PSP model and real transistor. Table lookup models called empirical models was implemented on *MATLAB* in the form of matrix containing device data for different bias points, were needed to evaluate real transistor. In this paper, a dimensioning of intrinsic gain stage based on g_m/I_d methodology using semi-empirical an EKV model was introduced.

The remainder of the paper was organized as follows. Section III presented the EKV formulation, comparative study with the PSP model was achieved. In Section IV, the validity of EKV model according to real transistor was reviewed. Section V presented the application of g_m/ I_D methodology on intrinsic gain stage dimensioning. Conclusions were drawn in section VI.

III. THE EKV3.0 MODEL

A. Presentation and formulations

The compact EKV 3.0 model was designed to simplify the MOS transistors dimensioning in advanced analog IC designs. It provides analytical, continuous, and physically correct description of weak, moderate and strong inversion including linear and saturation operation. The EKV3.0 MOS transistor has a hierarchical design, built through successive steps considering the major physical effects that may influence the transistor operation.

The EKV model Formulations rely on three basic parameters: The slope factor n, the specific current I_S and the threshold voltage V_{T0}. The latter is defined as the channel voltage for which the inversion charge becomes zero in the assumption of a strong inversion. The main equations constituting the model are given below.

The expression of the specific current is given by:

$$I_S = 2n(U_T)^2\mu C'_{ox}\frac{W}{L} = 2n(U_T)^2\beta \quad (1)$$

where the normalized drain current $i=I_D/I_S$.

The relation between the normalized drain current and the normalized mobile charge density and vice-versa is given by:

$i=q^2+q$ (2.1) $\quad q = 0.5\left(\sqrt{1+4i}-1\right)$ (2.2) (2)

The following expression relates the channel voltage V on the one hand and the normalized mobile charge density and the pinch-off voltage V_P on the other:

$$\frac{V_P - V}{U_T} = \left[2(q-1)+\log(q)\right] \quad (3)$$

Finally, the pinch-off voltage in EKV is computed as:

$$V_P = \frac{V_G - V_{T0}}{n} \quad (4)$$

where V_G and V_{T0} represent respectively the gate voltage and the threshold voltage.

Opposite to most MOSFET models, the EKV model made use the inherent symmetry of the MOSFET by referring all the terminal voltages to the substrate. Thanks to the device symmetry, the normalized drain current boils below to the difference between a forward component i_F and a reverse component i_R representing the drain current of saturated MOS transistors which source voltages are respectively V_S and V_D:

$$i=i_F-i_R \quad (5)$$

The graphical interpretation of EKV model presented by "Fig. 1" illustrates the drain current delivered by a saturated grounded source transistor whose parameters n, $V_{T0}$and I_S are considered respectively equal to 1.2, 0.4 V and 0.7A with three distinct values of gate voltage.

The corresponding pinch-off voltages predicted by "(4)" are marked by circles.

The $V_T(V)$ curves are plotted in a logarithmic scale proceeding by evaluating the non-equilibrium voltage V for every Vp by means "(3)".

The hatched areas identify $2nU_T^2i$ term that represent the drain currents divided by beta owing to the definition of I_S given by "(1)".

The gate voltage can be noticed to be large 0.6 V, the pinch-off voltage is positive, which is typical of a strong inversion. For $V_G<V_{T0}$ the pinch-off voltage V_P shifts left to become negative and the drain current decreases exponentially.

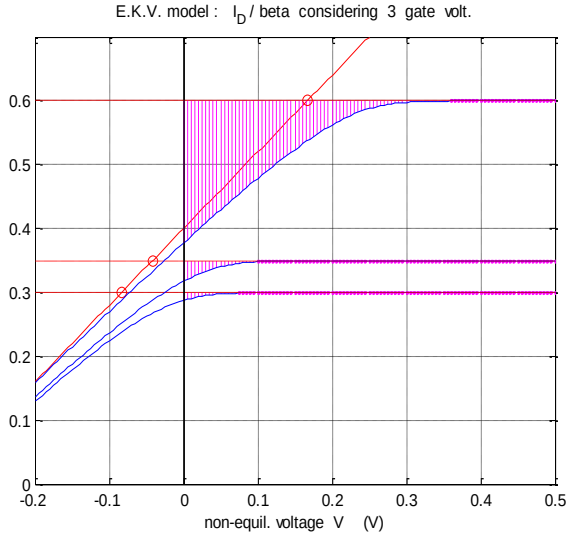


Fig. 1. Graphical illustration of drain current

B. Checking the EKV model against the PSP

In this part, the currents evaluated using the compact model were compared to the currents predicted by the PSP. First, the acquisition algorithm advocated in [3][5] has to be set up by MATLAB to extract n, I_S and V_{T0} from the PSP currents. Second, the currents by means of the E.K.V model have to be reconstructed and have to be compared to the new findings so as to check the validity of the new model.

Taking as a reference the original data, a unary N-type transistor having technological parameters issue from 0.18 µm CMOS process of TSMC technology was considered: An oxide thickness equal to 4.08nm, a substrate impurity concentration of 1.6 10^{17} cm-3 , and a V_{FB} =1 V. The temperature is 300°K.

Two distinct source voltages were selected; one for a weak inversion and the other for a strong one. The gate-to-substrate voltages from 0.6 to 1.8 V in steps 0.2 V was considered to be wide. After running the acquisition algorithm the value of unary specific current is I_{Su}=6.0476 10^{-007}A. The slope factor and the threshold voltage are 1.1227 and 0.0337, respectively.

"Fig.2" compares the reconstructed drain currents by means of the E.K.V model to the original PSP currents. The continuous lines represent the C.S.M. drain current and the circles stand for the strong and weak inversion. From the results illustrated in "Fig.2", the E.K.V compact model is remarked to be a good approximation of the PSP model.

In the following part, g_m/I_D ratios predicted by the compact model and the PSP were compared considering various back-bias voltages. An analytical expression of the g_m/I_D ratio in terms of the EKV compact model is given by [3]:

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\frac{q}{i} = \frac{1}{nU_T}\frac{1}{q+1} \qquad (5)$$

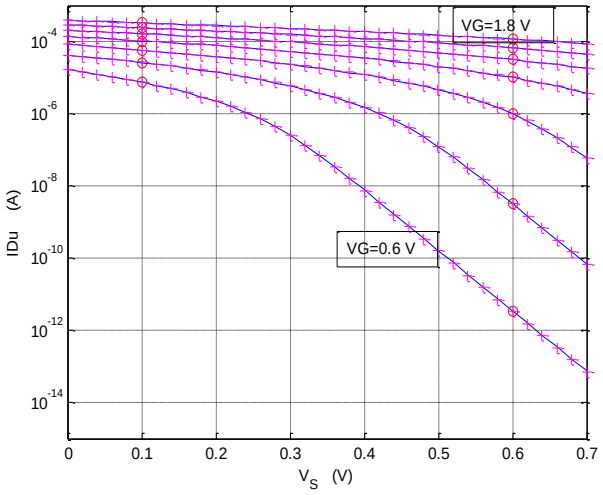


Fig. 2. Comparison between the reconstructed drain currents by Means of the E.K.V model and the original PSP currents

For the PSP, these were evaluated numerically by taking g_m/I_D the derivative of the log of the drain current. In "Fig. 3", the continuous lines represent the g_m/I_D ratios of the Charge Sheet Model. The crosses show the reconstruction based on the EKV model.

"Fig. 3" illustrates that the correspondence is satisfactory except for deep in weak inversion and low back-bias voltages. This might be due to the fact that the compact model does not consider the slight decrease of the subthreshold slope in a weak inversion.

The basic EKV model considered in the previous part was not suitable for real transistors, mobility degradation and short channel effects were ignored.

IV. The Real Transistor

In this part, we showed the impact of the gate length on the EKV model basic parameters in order to predict the drain currents and g_m/I_D ratios of real transistors. The only drawback was the introduction of look-up tables that contain a huge quantity of values extracted from the empirical model.

A. The inflence of the gate length on the model parameters

The gate length brings up the issue of some well-known effects, such as threshold voltage roll-off, reverse short channel effect, DIBL and CML.

Fig. 4" illustrates the impact of the gate length on the slope factors of N- and P-channel transistors, the threshold voltage and the specific current I_S.

Below 1µm, the threshold voltage starts to increase progressively at short gate lengths. The global increase, called the reverse short channel effect. In addition, "Fig. 4" illustrates that the specific currents increase slightly when the drain voltage increases. The effect is commonly designated by the acronym CLM for Channel Length Modulation.

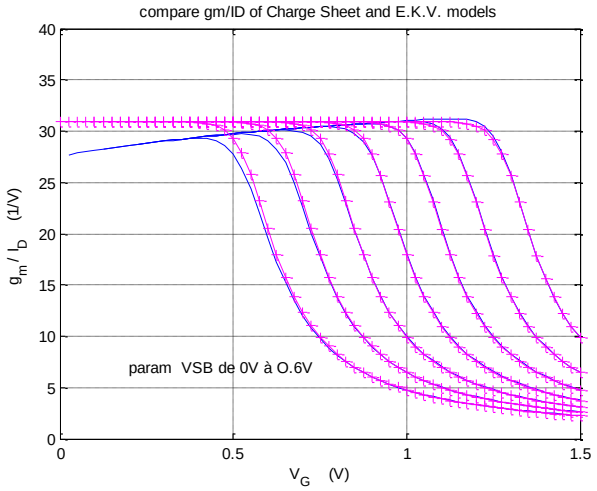
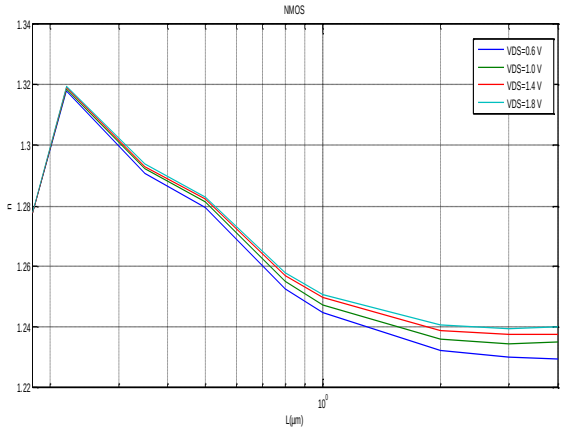
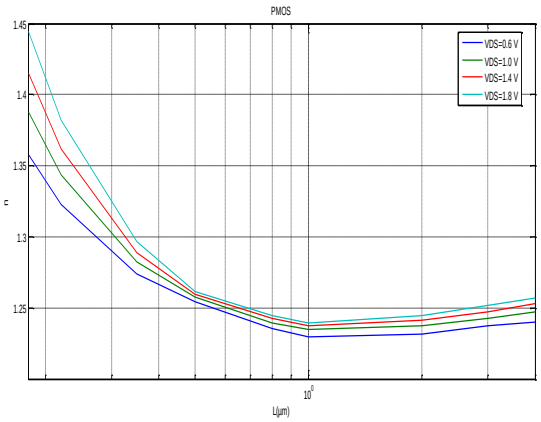


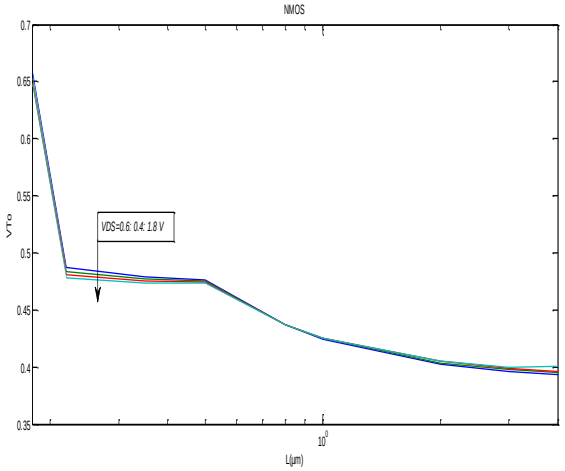
Fig. 3. Comparison between the reconstructed the gm/ID ratio by means of the EKV model to the original PSP considering various back-bias voltages



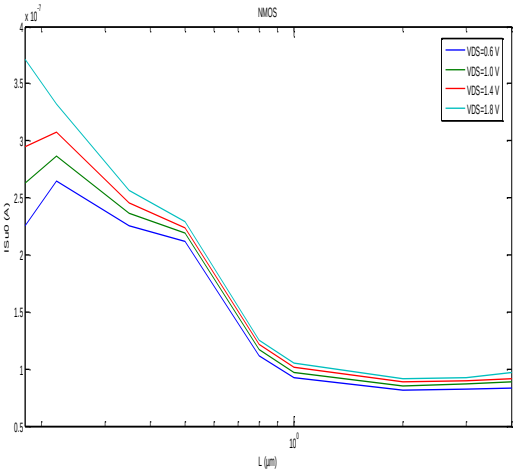
(a) n versus L for N-channel transistor



(b) n versus L for P-channel transistor



(c) V_{T0} versus L for NMOS transistor



(d) I_{SU0} versus L for NMOS transistor

Fig. 4. Plot of the slope factors of N- and P-channel transistors, threshold voltage and the specific current I_S versus the gate length considering four equally spaced drain voltage comprised between 0.6 and 1.8V

B. *Checking the validity of EKV model when its parameters vary with the source and drain voltages*

"Fig.5" displays a sample that shows the drain currents of a 10 µm wide N-channel MOS transistor whose drain-to-source voltage varies from 0.6 to 1.8 V, considering two gate lengths (0.18 µm and 1µm). The device belongs to a 180 nm technology developed by TSMC and consists of look-up tables listing the empirical data and implemented with MATLAB on an organized cell.

In this part, the EKV model was used to reconstruct I_D versus V_{DS} characteristic benefiting from the parameters that depend on the source and drain voltages including hort channel devices impact discussed previously.

Finally, the drain currents predicted by the model were compared to real I_{DS} (V_{GS}) characteristics. To this end, the identification algorithm presented by [5] is needed in order to extract the basic EKV parameters from empirical data achieved on real physical transistors.

"Fig 6" shows the reconstructed drain currents obtained by means of the EKV model.

The drain currents (dots) are compared to those of "Fig 5" (plain lines). As for the dashed lines, they relate to the model when the mobility is supposed to be invariant.

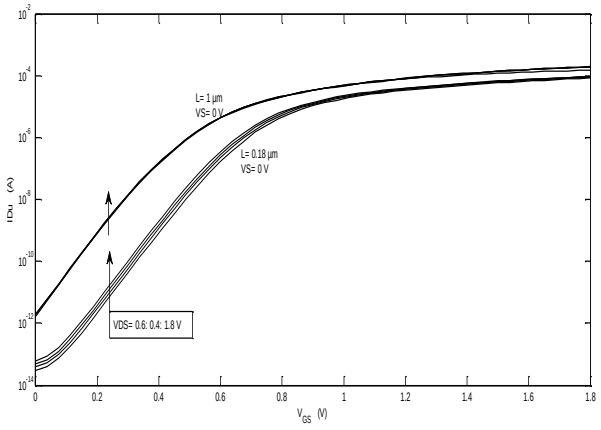


Fig. 5. Drain currents of an N-channel unary transistor. The device belongs to a 180 nm technology developed by TSMC

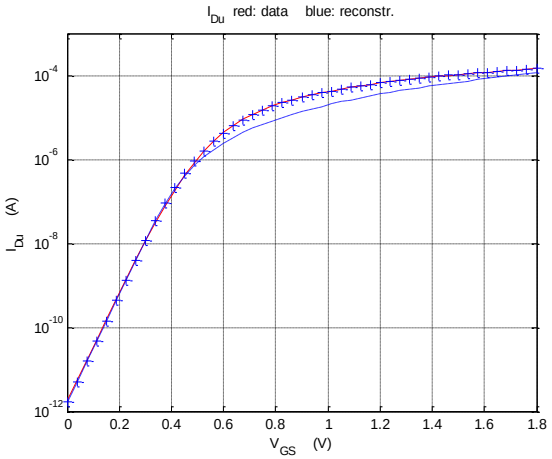


Fig. 6. Comparison between reconstructed drain currents (dots) by means of EKV model to the currents of "Fig. 5" (plain lines)

The assumption that the reconstructed currents agree fairly well with the physical currents is accepted implicitly. The model reproduces reasonably well real I_{DS} versus V_{GS} characteristics.

The extension of the E.K.V model to short channel devices considered in previous part lays down the foundation for the sizing of elementary amplifier.

V. Sizing the Elementary Amplifier

A. The elementary amplifier

The circuit of elementary amplifier called currently the 'Intrinsic Gain Stage' (IGS), shown in "Fig. 7", consists of a saturated common source transistor loaded by a capacitor.

We therefore consider the small signal equivalent circuit shown in "Fig. 8".

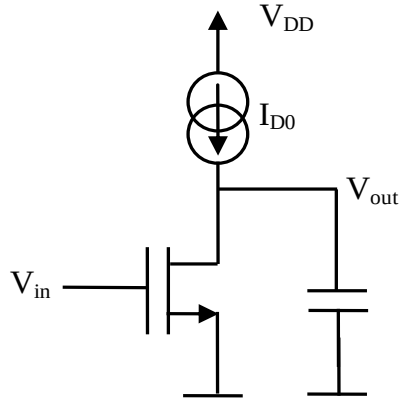


Fig. 7. Elementary amplifier

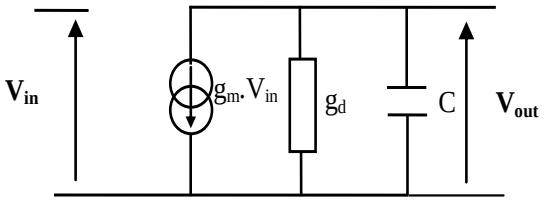


Fig. 8. Small signal equivalent circuit of elementary amplifier

In this section the sizing method of the elementary amplifier based on EKV model was reviewed by means of the g_m/I_D methodology. Our aim was to calculate gate width and drain current optimum values to control the circuit performance and achieve a desired gain-bandwidth product.

The DC gain is given by:

$$|A| = \frac{g_m}{g_d} = \frac{g_m}{I_D} \cdot \frac{I_D}{g_d} = \frac{g_m}{I_D} \cdot V_A \quad (6)$$

where V_A represent the early voltage

The relation between transconductance g_m and transition frequency f_T is given by:

$$g_m = 2\pi \cdot f_T \cdot C \quad (7)$$

The g_m/I_D methodology benefits from the variation of the transconductances and drain currents with the gate width where the key term g_m/I_D ratio is independent of the gate width and offers the possibility to achieve the transconductance derived from the expression below and deduce the gain bandwidth product.

The g_m/I_D ratio can be set up using two strategies. The first makes use of experimental $I_D(V_{GS})$ characteristics carried from measurements on real transistors. This is called the semi-empirical g_m/I_D sizing method. The other method refers to the analytical expressions for g_m/I_D founded in EKV model formulations.

Before applying the semi-empirical g_m/I_D method to size the elementary amplifier, let us look at the dependence of g_m/I_D on the gate-to-source and drain-to-source illustrated in "fig. 9".

For a desired transition frequency fixed at 100MHz, a MATALB computation is developed illustrating a contour plot of intrinsinc gain shown in "fig.10".

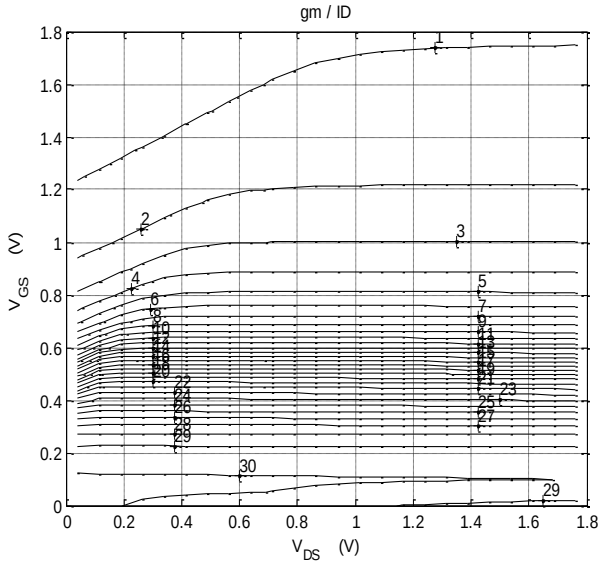


Fig. 9. gm/I_D contours versus drain an gate voltages for 0.18 µm gate length of NOMS transistor

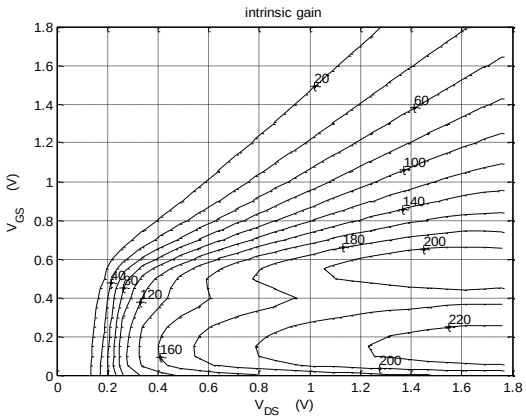


Fig. 10. Intrinsic gain contours versus drain and gate voltages

A series of gate widths, gate voltages V_{GS} and gains achieving the desired gain-bandwidth product is displayed in "Fig. 11" considering four drain voltages V from 0.25 to 1 V.

"Fig. 12" shows the impact of the gate length on the gate width, gate-to-source voltage and gain when L takes the following values 0.18, 0.5 and 0.22 µm.

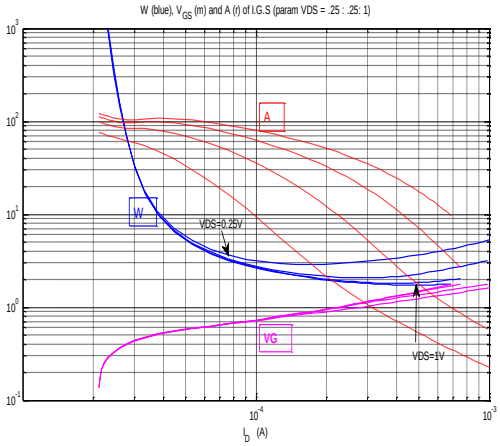


Fig. 11. Plot of the gate widths W, V_G(V) and gain A versus drain current for transistor frequency equal to 100 MHz

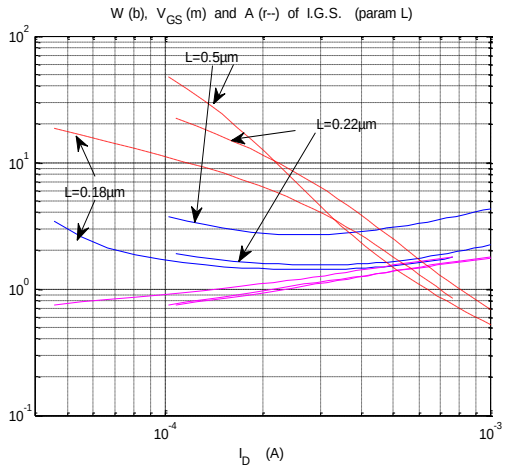


Fig. 12. Illustration of the influence of the gate length

B. The sizing procedure

In this subsection, sizing was undertaken considering the compact model instead of 'semi- empirical' data. It is divided into two parts: first, W and I_D were evaluated and then the Intrinsic Gain A was estimated.

Implemented on MATLAB, the sizing algorithm begins with the extraction of the model parameters from the empirical model. A q_F logspace vector that encompasses the moderate inversion region was then defined. This leads to the estimation and evaluation of the pinch-off voltage and the normalized reverse mobile charge density vector q_R. In a last step, the normalized drain current i was extracted.

In "Fig. 13" the width, gate-to-source voltage and intrinsic gain predicted by the model (continuous lines) are compared to their semi-empirical counterparts (crosses). The gain-bandwidth product is equal to 1 GHz and the output capacitor to 1 pF.

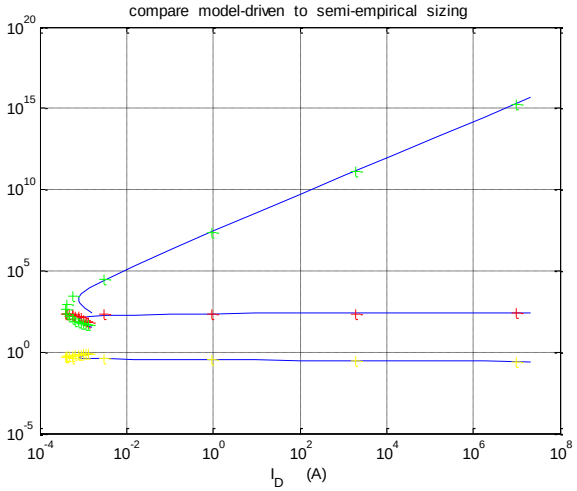


Fig. 13. Comaraison between W, A and V_{GS} predicted by EKV model (continuous lines) and its semi-empirical counterparts (crosses)

Considering the compact and the semi-empirical models, the sizing results are similar in most of the operation regions. Therefore, one of the important benefits of EKV model procedure is that the sizing can be achieved in well defined regions.

VI. Conclusion

This paper proved the consistency of the EKV3 model when describing the real transistor of 180 nm MOSFET technology. Extraction of EKV parameters algorithm was done using MATLAB. The results bring about a number of interesting observations highlighting the impact of the short channel effects on the parameters of the compact model. For a long and short channel transistor, the observed modeling result in weak, moderate and strong inversion cover qualitatively well all the aspects of the MOS transistor.The simplicity of the model has allowed us to reach a performing sizing of real Intrinsic Gain Stage. This underlines the suitability of the EKV3.0 model to be usefully used in analog circuit design for several applications such as OTA circuit and Ring VCO. Such a study is the topic of our future potential perspective.

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