Design of Modulator and Demodulator for a 863-870 MHz BFSK Tranceiver

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***Abstract*—This paper presents the design of low power modulator and demodulator circuits dedicated to a BFSK transceiver, operating in the 863- 870 MHZ ISM band. The two circuits were designed using ams 0.35µm technology with 3V dc voltage supply. Simulation results of the new Direct Digital Frequency Synthesizer in the modulation have shown good performances of the designed system as the Spurious Free Dynamic Range SFDR reached -88 dBc while the circuit consumes only 47.7 µW @ 43.3MHz. The demodulator has also presented a good BER of 10^{-3} @10.9 EbtoN0 and a sensitivity of about -115 dBm.**

Keywords—ISM band; FHSS; FSK modulator; BFSK demodulator; wireless sensor network

I. Introduction

The low-power market has experienced explosive growth over the past ten years by the presence of new wireless command and control technologies. This expansion is provided by the technology of wireless sensor networks of low range, which has many applications including home automation, industrial and commercial automation, peripherals for personal computers but also medical survey and health care monitoring. Actually, the requirement for vital sign monitoring has significantly increased as population aging is rapidly progressing in many industrialized countries. This grow-up is accompanied by an even more dramatic increase in the number of old people suffering from chronic diseases and disabilities as specified in [1].

Thus, several standards have been studying the implementation of wireless sensor network, such as the ultra wideband UWB (IEEE 802.15.3) standard [2], Bluetooth (IEEE 802.15.1), but mostly the standard Zigbee (IEEE 802.15.4) that is dedicated to the wireless networks of the family WPAN LR (Low Rate Wireless Personal Area Network) [3]. Therefore we propose to design a wireless sensor that will be integrated in a wireless sensor networks used for vital sign monitoring using the Zigbee protocol. The RF transceiver will operate in the 863-870 MHz ISM band, as it is available only in Europe, so presents a good field for testing new concepts in order to develop low power transceiver for short range and low data-rate applications.

As the direct conversion transceiver has shown interesting specifications like low power consumption and low manufacturing costs [4], this architecture is used for the wireless sensor.

In this paper, the design of two blocks in the transceiver is presented. A new method for FSK (Frequency Shift Keying) modulation is presented using binary scheme modulator and transistor level of a zero crossing demodulator is then realized using 0.35µm technology. The paper is organized as follows: section II describes the FSK transceiver architecture, section III presents the design and implementation of the digital modulator while section IV details the design of the digital demodulator. Finally simulation results are presented in section V and a conclusion and perspectives are given in section VI.

II. Tranceiver Architecture

The Frequency Shift Keying (BFSK) transceiver is presented in Fig.1. The BFSK modulator uses a Frequency Hopping Spread Spectrum (FHSS) technique and a Direct Digital Frequency Synthesizer (DDFS), which allows the generation of BFSK signal using hopping frequencies. Hence the digital data is synthesized in quadrature outputs signals in base band and up converted to the center frequency of the ISM band using a single-sideband up conversion mixer controlled by a local oscillator that selects either the lower or the upper sideband for the instantaneous carrier frequency.

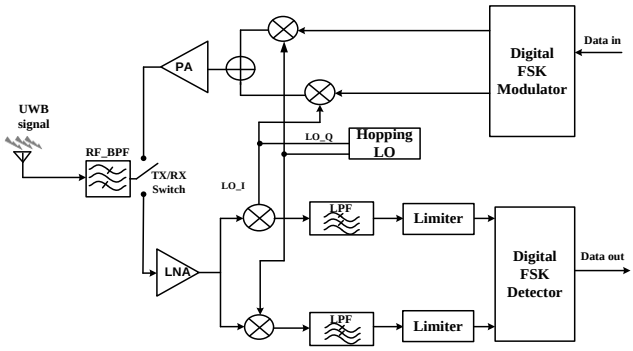

Fig. 1. Transmitter architecture

The transmitted data is carried by symbol tones at an offset of ±20 kHz from the carrier frequency, so a maximum data rate of 20 kb/s is achieved by sending two symbols per hop. Received by the antenna, the signals concourse a bandpass filter that selects the ISM band, then a low noise amplifier (LNA) which provides enough power for the signals to spread with a minimum noise.

As the ISM Band is composed of several channels, the operating one will be selected using a low pass filter followed by a limiting amplifier to convert the received signal into binary level [5], instead of using a linear and complicated

automatic gain control, as in most FM receivers. Finally the correct transmitted data will be at the output of a digital FSK Detector.

III. Design of the Digital FSK Modulator

A. Modulator Specifications

In order to select the appropriate Data rate, it is necessary to estimate the overall average power consumption of a transmitter node in the sensor networks. A thorough study in [6] has given an approximated formula for the power dissipated by the transmitter as a function of the data rate. The result is in Fig.2 and show that a data rate of 20 kb/s is selected taking into account the requirements of lower power, a BFSK tone frequency to avoid the impact of DC offset and flicker noise caused by direct conversion architecture and bandwidth efficiency.

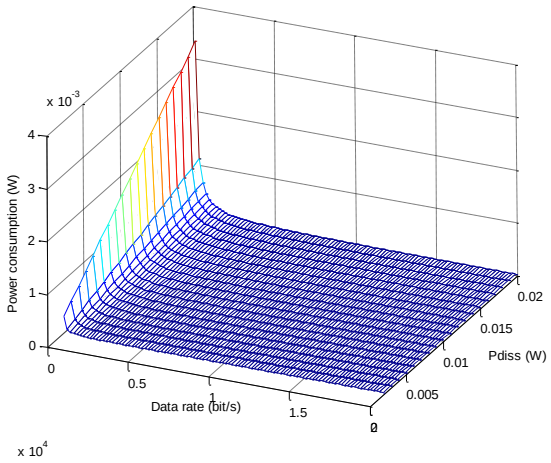

Fig. 2. Transmitter power consumption as a function of data rate and node power dissipation

As the ETSI (European Telecommunications Standards Institute) regulations require a minimum separation of 25 KHz bandwidth between two adjacent channels, and in order to follow the requirement of FHSS technology, the ISM band 863-870 MHz was divided into 58 channels with a transmission bandwidth of 80 KHz for the each transmitted signals and a separation of 40 KHz between adjacent channels. The power spectrum of a BFSK signal is reported in Fig. 3.

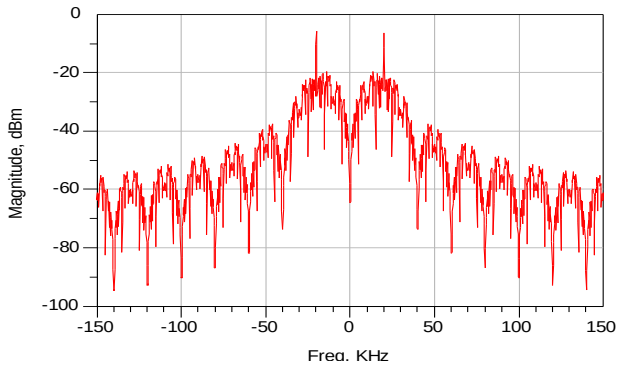

Fig. 3. Power spectrum of a BFSK signal (bit rate=20Kbps)

B. Modulator Implementation

The proposed architecture of the modulator circuit is presented in Fig.4. It is composed of a DDFS, a PN code generator and a multiplexer. The role of the DDFS is to produce digital samples from baseband sinusoidal waveforms by addressing a sine ROM (Read Only Memory) at a frequency set by a 20-bit control sequence. The PN code however, generates a random code corresponding to the hopping pattern and among which, the multiplexer will select a single code [7].

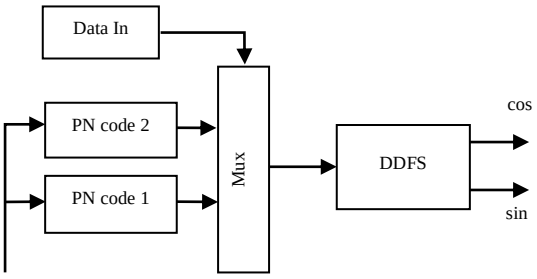

Fig. 4. Block diagram of the modulator

A minimum clock speed Fclk of 43.4 MHz was used in this modulator system, thus a smallest frequency resolution of about 41.29 Hz is obtained since the frequency control word is 20 bits fixing the frequency control resolution Fr to 41.29 Hz as:

$$F_r = \frac{F_{clk}}{2^N} \quad (1)$$

Where F_{clk} is the sampling frequency of the DDFS/DAC and N is the number of frequency control bits.

Fig.5 shows a typical architecture of a DDFS system, it is mainly composed of a phase accumulator, a sine/cosine generator and a ROM.

At each edge of the clock the PN code generates a word binary N that is used to increment the phase accumulator in the DDFS, and every N binary word will be carried in a ROM memory, as shown by the VHDL test simulator in Fig.6.

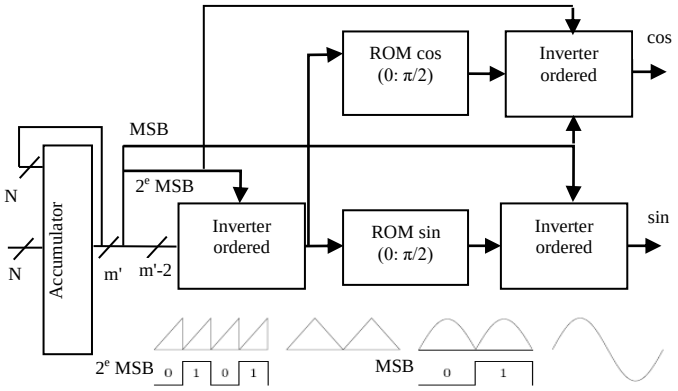

Fig. 5. Architecture of DDFS system

The length of the internal word also ensures a spurious tone of at least -72.6 dBc from the fundament frequency freeing therefore the imperfections in the DDFS [8].

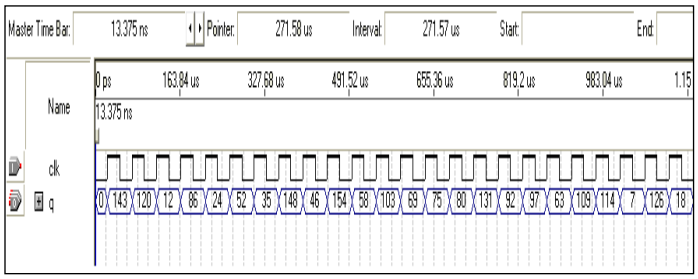

Fig. 6. PN code Simulation results

The bloc diagram of the phase accumulator is depicted in Fig.7. Generally this circuit is pipelined as m stages of L bits each as: m×L=N [7].

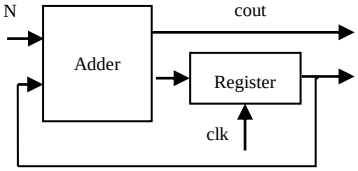

Fig. 7. Block diagram of the phase accumulator

IV. Design of the Digital FSK Demodulator

The digital demodulation is realized using a limiter that converts the received analog signals into binary levels and a zero crossing BFSK detector.

A. Design of the limiting amplifier

The limiting amplifier has a cascaded architecture. Indeed, the number of cells used, the amplification gain, the bandwidth and the consumption of each cell determine the overall performance of the circuit [9].

In order to determine the number of stages that may be used for this application, simulations of the total gain GT and bandwidth BT variations were carried (Fig.8) considering a number Z of identical cells for the whole limiter [10] as:

$$\text{Gain of each cell:} \quad G_C = G_T(^1/_Z) - 1 \tag{2}$$

$$\text{Bandwidth of each cell:} \quad B_C = \frac{1}{\sqrt{2^{1/Z}-1}} \tag{3}$$

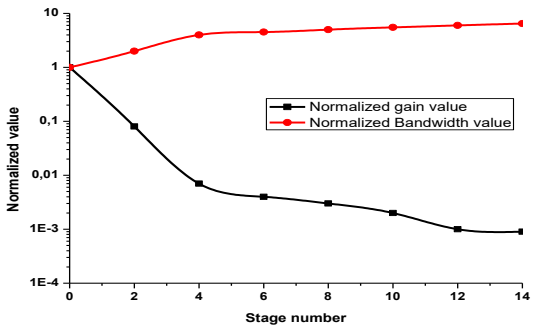

Fig. 8. Variation of gain and bandwidth based on the number of cells

Also the total power consumption of the circuit depends on the number of stages used as:

$$P_T = Z \times (G_C \times B_C)^2 \tag{4}$$

Thus, the number of limiting amplifiers has to be reduced so to meet the requirements of low consumption for the intended medical application. A compromise between the different specifications has led to the use of 7 floors of limiting amplifiers which a cell is shown in fig.9.

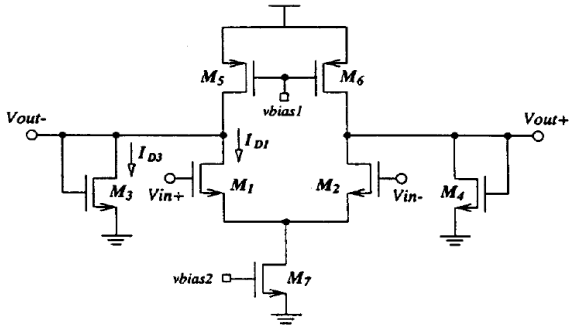

Fig. 9. Proposed limiting amplifier

The circuit is composed of a conventional simple source coupled pair [11] with a load diode biased with an independent current.

B. Design of the BFSK demodulator

The designed demodulator is shown in Fig.10. It is composed of four differentiators circuits which detect the zero crossing of I and Q signals at the output of the limiter, two OR gates and one NOR gate, a shape keeping circuit and a low pass filter.

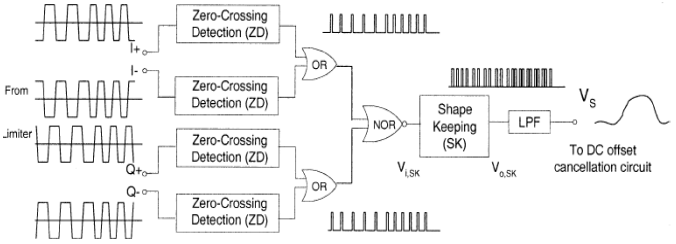

Fig. 10. Architecture of the proposed BFSK demodulator

The architecture of one ZD circuit is given in Fig.11. For every zero crossing of the input signal, the circuit generates a pulse whose width depends of the circuit component values as:

$$\tau = (R.C)Ln(2) \tag{5}$$

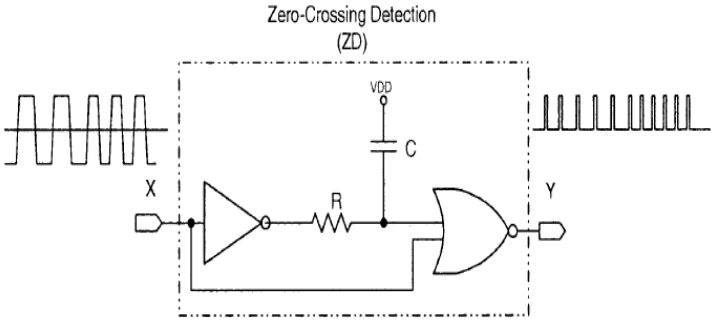

Fig. 11. Zero-crossing Detection

As the output generated pulses don't have the same width as shown at the output in Fig.11, after the collection with the logic OR and NOR gates, a shape keeping circuit (Fig.12) is utilized to fix the width of every input pulse whose value depends on the parameters of the circuit components. Indeed the width is mainly determined by the ratio of the R1-R3 voltage divider and the values of the capacitor C2 and the resistor R5 at the drain of the output transistor.

Finally a digital low pass filter is applied to the generated pulses so to filter errors and to calculate the mean value of the signals which allow determining whether it is a 0 or 1 transmitted Data. The cut-off frequency of the filter is equal to 80 KHz which is exactly the width of a single channel in the ISM band 863-870 MHz. The filter response is shown in Fig.13.

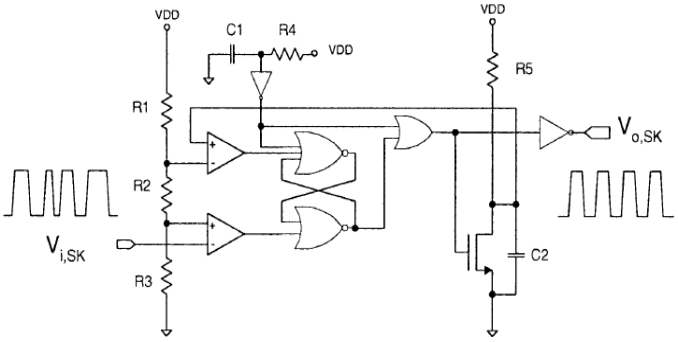

Fig. 12. The Shape keeping circuit

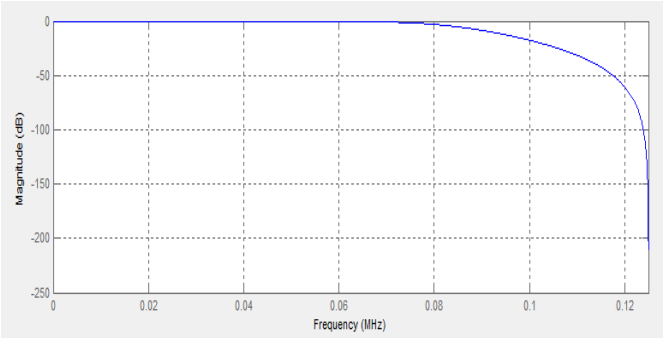

Fig. 13. Digital filter response

V. Simulation Result

The modulator simulation is first achieved with Modelsim in VHDL language, then the code was synthetized using Quartus and a chip of the whole cicuit was realized using Cadence. Fig.14 shows the simulation of VHDL maximum code of the modulator. At each edge of the clock (Clk), the PN code generates a word binary that increments the phase accumulator of the DDFS, and for each increment in this DDFS (clk2), the modulator outputs sample of sin and cos signals. Moreover, The multiplexer switches between the two PN code at each edge of the signal (s).

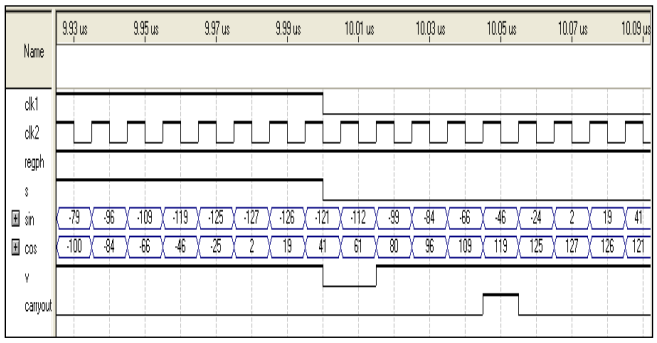

Fig. 14. Maximum code vhdl simulations

Fig.15 shows the output sine and cosine signals of the modulator. Indeed, a quadrature phase is observed between the two signals as if the sine is at its maximum, the cosine takes negative values and if it is at zero, the cosine takes its maximum.

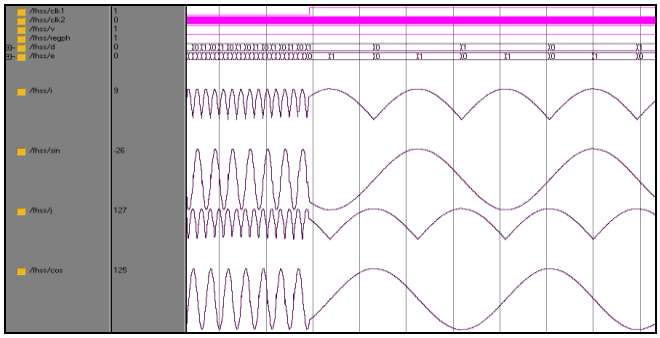

Fig. 15. Modulator Block simulation results

The chip implementation of the modulator circuit is shown in Fig.16. It was realized using ams 0.35µm CMOS standard cell library. The chip design was divided into thirteen subsystems and simulations results have shown that the average power consumed by the whole circuit is about 47.7 µW at Fclk=43.4 MHz and the Spurious-Free Dynamic Range is about -88 dBc which complies with the specifications of the ISM band.

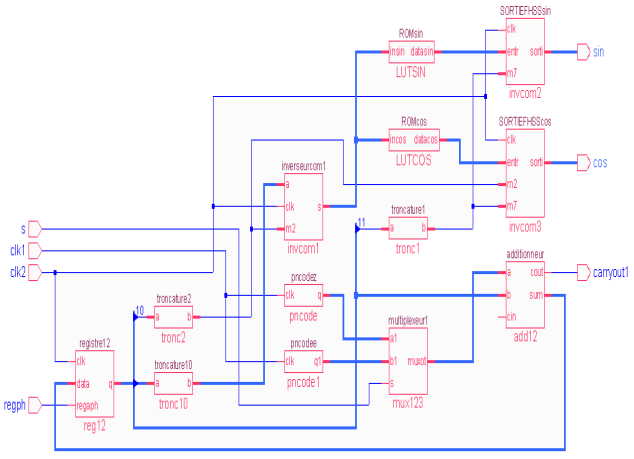

Fig. 16. Chip design

The BFSK signals at the output of the modulator were applied to the designed demodulator using an Additive White Gaussian Noise (AWGN) channel. Thus, the diagram of Fig.16 was obtained including the input data of the modulator (in blue), the output of the filter at the end of the demodulator (in red) and the data out (in pink) after integration and dump of the signals.

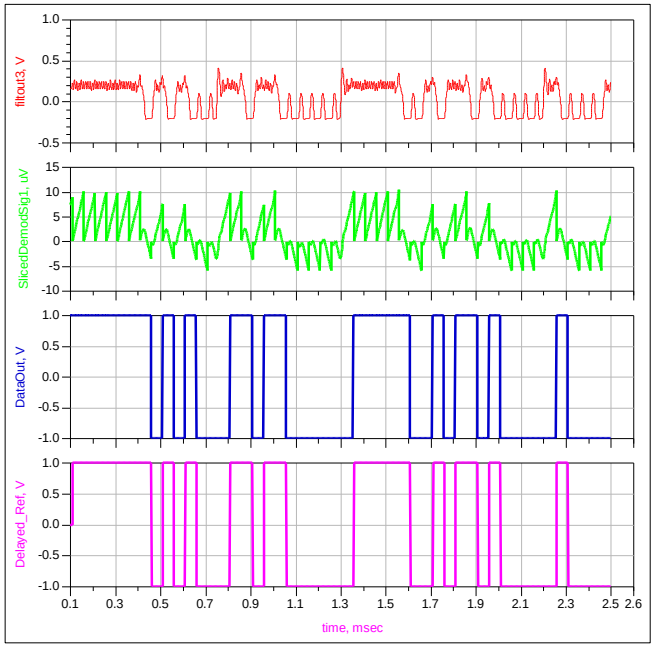

Fig. 17. Output signals of the demodulator

Finally a bit error rate simulation BER was achieved as a function of EbtoN0 expressing the signal to noise ratio performance. The result is in Fig.17 and shows that for a bit error rate of 10^{-3}, only 10.9 dB of the EbtoN0 is needed for the circuit which deeply satisfies the requirement of the application and the FSK modulation. The Demodulator circuit presents a sensitivity of about -115 dBm.

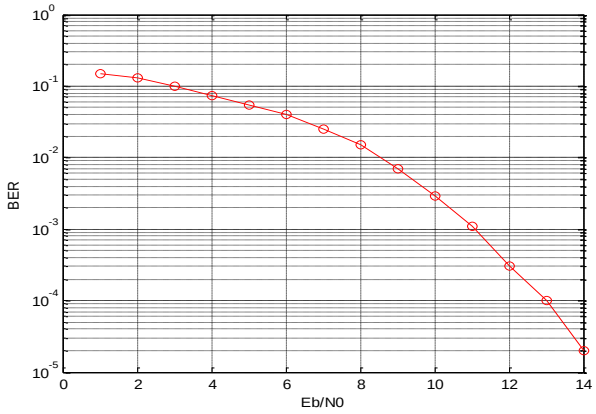

Fig. 18. BER plot versus EbtoNo(dB)

Performance comparison between the proposed modulator and demodulator circuits and other reported works in the literature are presented in table I and table II respectively.

TABLE I. PERFORMANCE COMPARISON OF THIS WORK (MODULATOR) AND REPORTED WORKS IN LITERATURE

	[12]	[13]	[14]	This work
Output (bits)	12	12	10	10
Fclk (MHz)	480	150	500	43.4
SFDR (dBc)	-80	-84	-70	-88
Power dissipation (µW/MHz)	72	500	34.4	47.7
Supply voltage(V)	2.5	1.8	1.8	3

TABLE II. PERFORMANCE COMPARISON OF THIS WORK (DEMODULATOR) AND REPORTED WORKS IN LITERATURE

	[15]	[16]	This wok
EbtoN0 (dB)	10.5	16	10.9
Sensitivity (dBm)	-114.5	-109	-115

VI. CONCLUSION

In this paper, a novel design and implementation of FHSS-FSK modulator and demodulator for a 863-870 MHz receiver was presented. First, we have presented a new method for designing the modulator exploiting the symmetry of trigonometric functions (sine and cosine) in order to reduce the spurious tones of the Direct Digital Frequency Synthetizer. Thus, a new architecture of the DDFS with small lookup table for the sine and cosine functions and pipelined phase accumulators was put into test. Simulation results showed that the designed modulator was able to generate BFSK signals with frequency hopping while consuming only 47.7 µV at 43.4 MHz.

A BFSK demodulator circuit was also designed using ams 0.35µm technology, the circuit was tested with input signals coming from the designed modulator bloc. Simulation results showed that the circuit presents 10^{-3} of bit error rate for an input signal to noise ratio of 10.9 DB while the sensitivity reached -115 dBm. Therefore, the designed circuits are suitable for FSK modulated applications as the health monitoring systems.

As a perspective of this work, we can achieve the design of the whole transceiver using the UWB technology and BPSK modulator as in [17], and compare the performances of the two designed works for a better use in this medical application.

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